LHCb RICH LS3 enhancements: introducing a novel fast-timing readout chain

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6th Workshop (Barcelona) on LHCb Upgrade II

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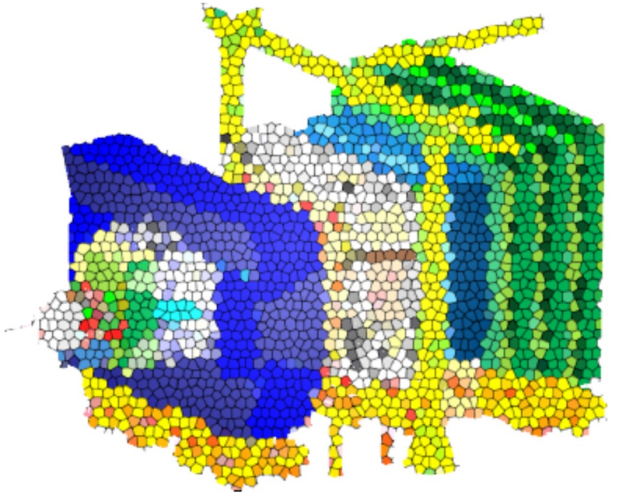
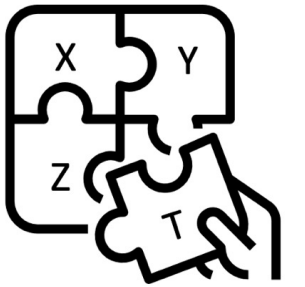


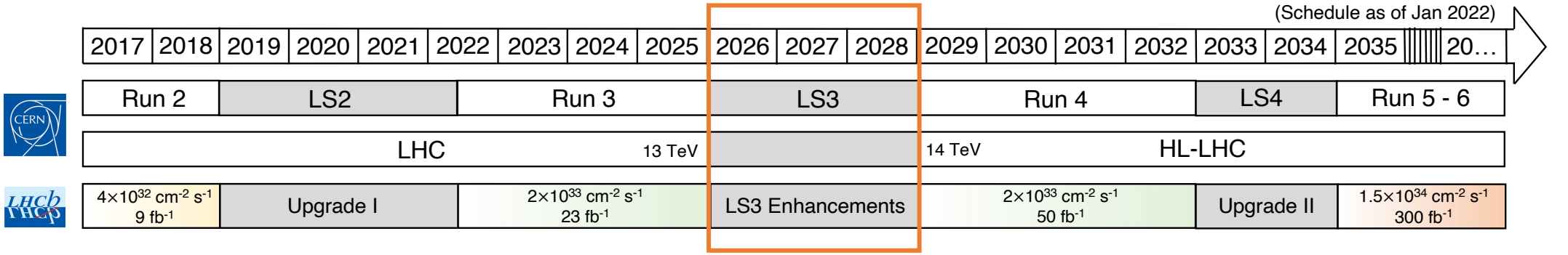
Motivation for LS3 enhancements

The LHCb RICH LS3 enhancements aim to equip the detector with new front-end readout electronics including the FastRICH ASIC capable of timestamping photon detector hits with ~ 25 ps time bins.



The LS3 enhancement will:

- Improve PID performance during Run 4.
- Provide a new fast-timing perspective to LHCb including a primary vertex time estimate.
- Give us important experience with fast-timing techniques in LHCb in preparation for Upgrade II.
- Enhance the detector at relatively favourable cost.
- Profit optimally from the 3 year period of LS3, central to the RICH evolution.



Introduction and TDR

Many details are included in the RICH LS3 proposal.

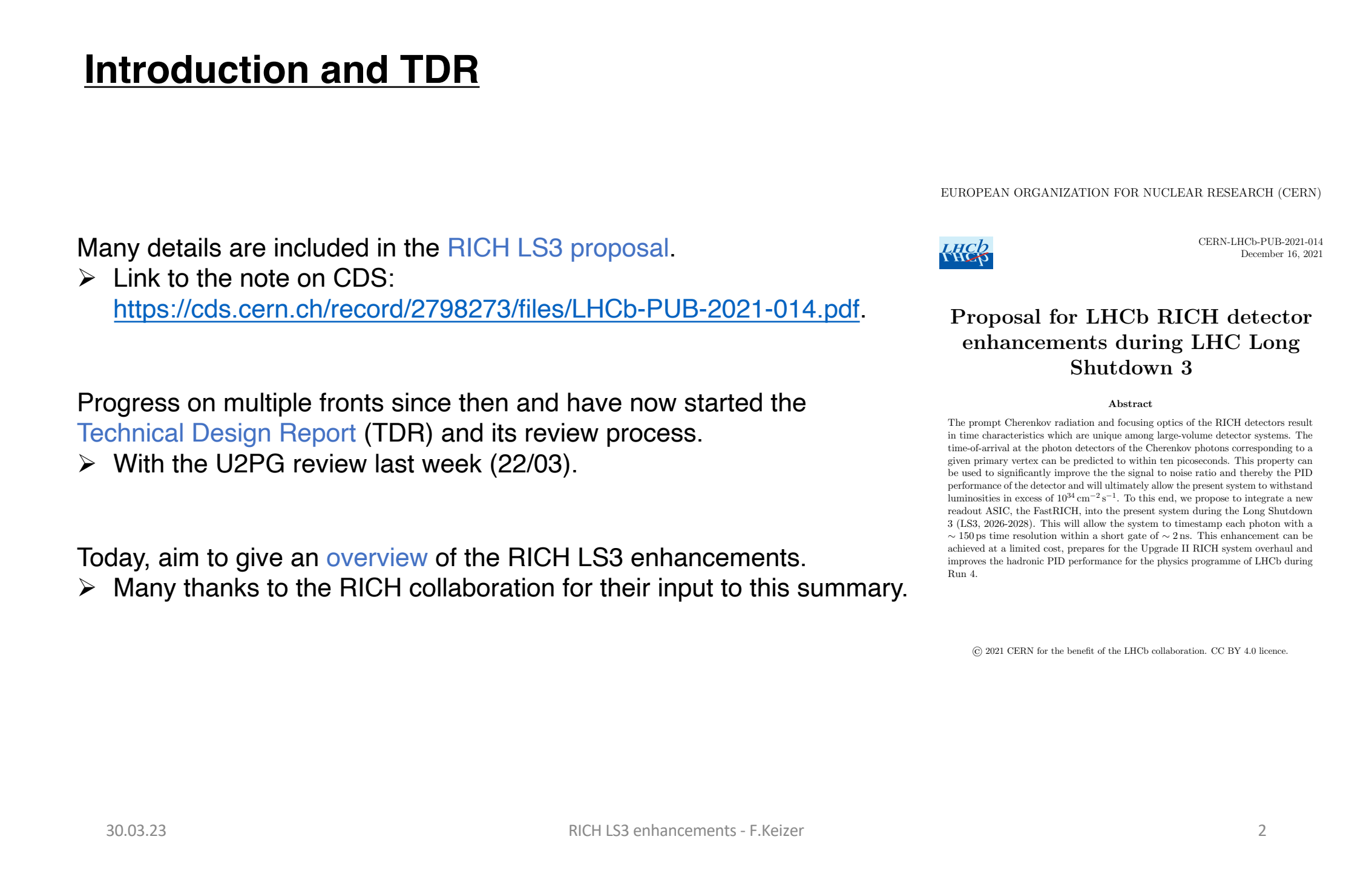
- Link to the note on CDS: https://cds.cern.ch/record/2798273/files/LHCb-PUB-2021-014.pdf.

Progress on multiple fronts since then and have now started the Technical Design Report (TDR) and its review process.

- With the U2PG review last week (22/03).

Today, aim to give an overview of the RICH LS3 enhancements.

- Many thanks to the RICH collaboration for their input to this summary.



EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH (CERN)

CERN-LHCb-PUB-2021-014
December 16, 2021

Proposal for LHCb RICH detector enhancements during LHC Long Shutdown 3

Abstract

The prompt Cherenkov radiation and focusing optics of the RICH detectors result in time characteristics which are unique among large-volume detector systems. The time-of-arrival at the photon detectors of the Cherenkov photons corresponding to a given primary vertex can be predicted to within ten picoseconds. This property can be used to significantly improve the the signal to noise ratio and thereby the PID performance of the detector and will ultimately allow the present system to withstand luminosities in excess of $10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$. To this end, we propose to integrate a new readout ASIC, the FastRICH, into the present system during the Long Shutdown 3 (LS3, 2026-2028). This will allow the system to timestamp each photon with a $\sim 150\,\mathrm{ps}$ time resolution within a short gate of $\sim 2\,\mathrm{ns}$. This enhancement can be achieved at a limited cost, prepares for the Upgrade II RICH system overhaul and improves the hadronic PID performance for the physics programme of LHCb during Run 4.

- **Recap: use of fast-timing information in Run 4.**
- New electronic readout chain.
- FastRICH ASIC.
- Power and cooling of an elementary cell.

RICH photon time-of-arrival distribution

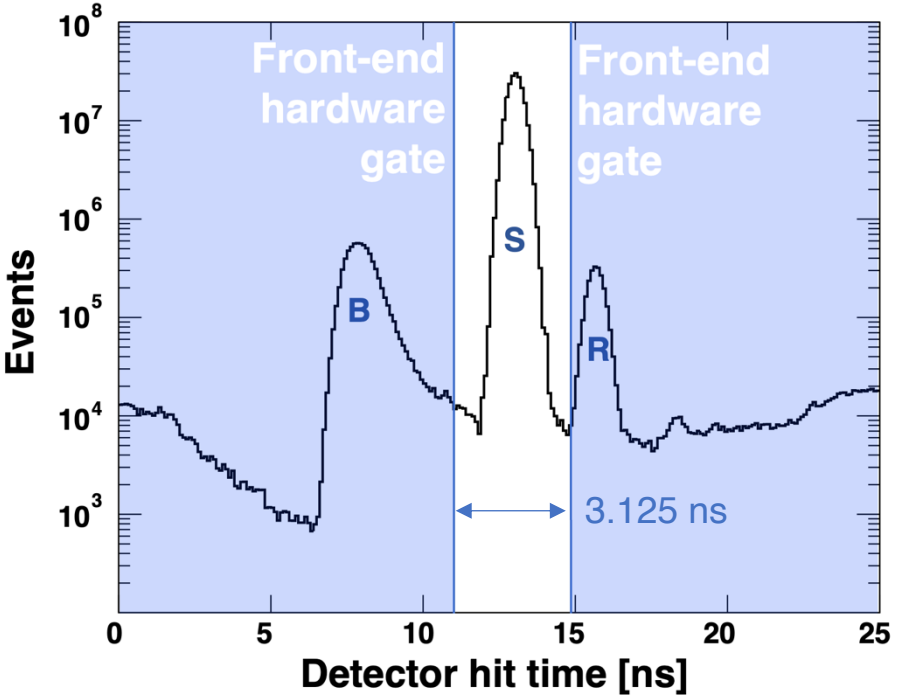
For a given track, the Cherenkov photons arrive simultaneously on the photon detector plane.

- Follows from prompt emission and focusing geometry.

However, looking at the distribution of many tracks across many bunch crossings, the signal peak labelled ‘S’ is spread across a few nanoseconds.

- Primary vertex time spread.
- Different track paths through the detectors.

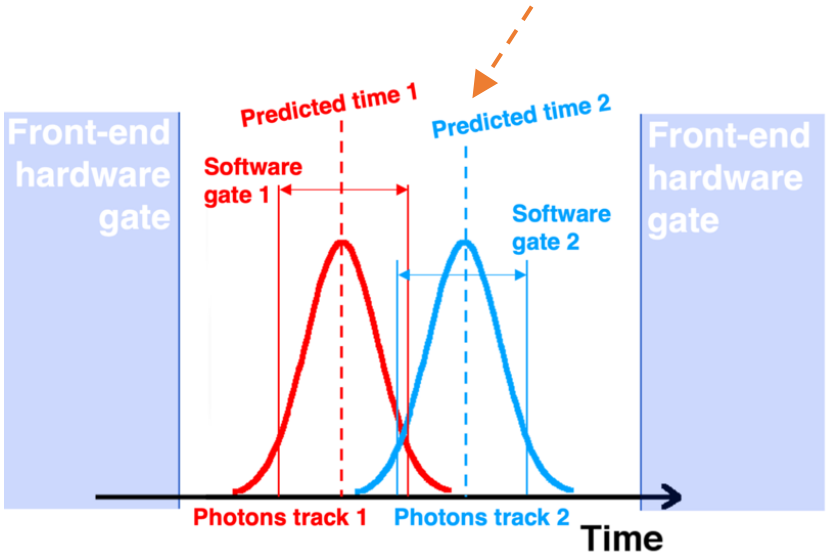
Without event reconstruction, the best time-based filtering is a few nanoseconds at the front-end: a “hardware time gate” to reduce data throughput to the back-end.

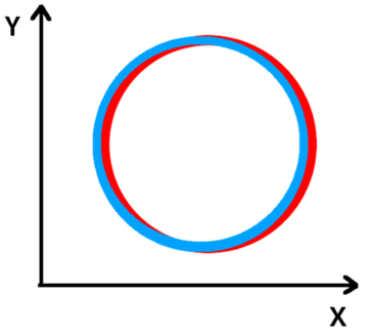


Time gate in the reconstruction software

Using the RICH reconstruction algorithms, for a given primary vertex (PV) start time, it can be accurately (picosecond-level) predicted when a photon is expected to arrive.

- For this we use the reconstructed track and photon path (*full equation in backup slide*).



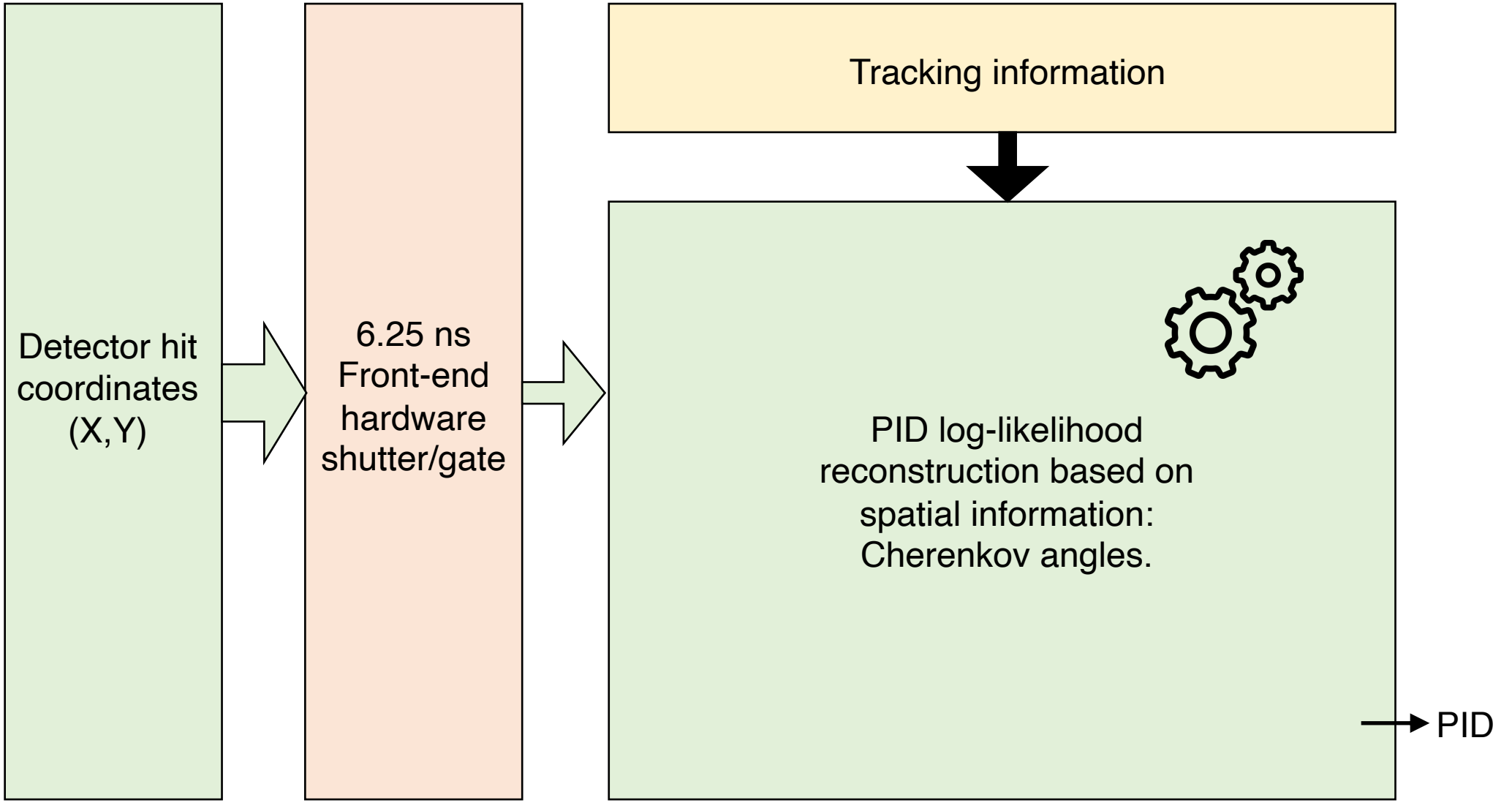


In the reconstruction software, only photons within a software time gate around the predicted time for the track are considered: strong reduction in combinatoric background of signal originating from different PVs.

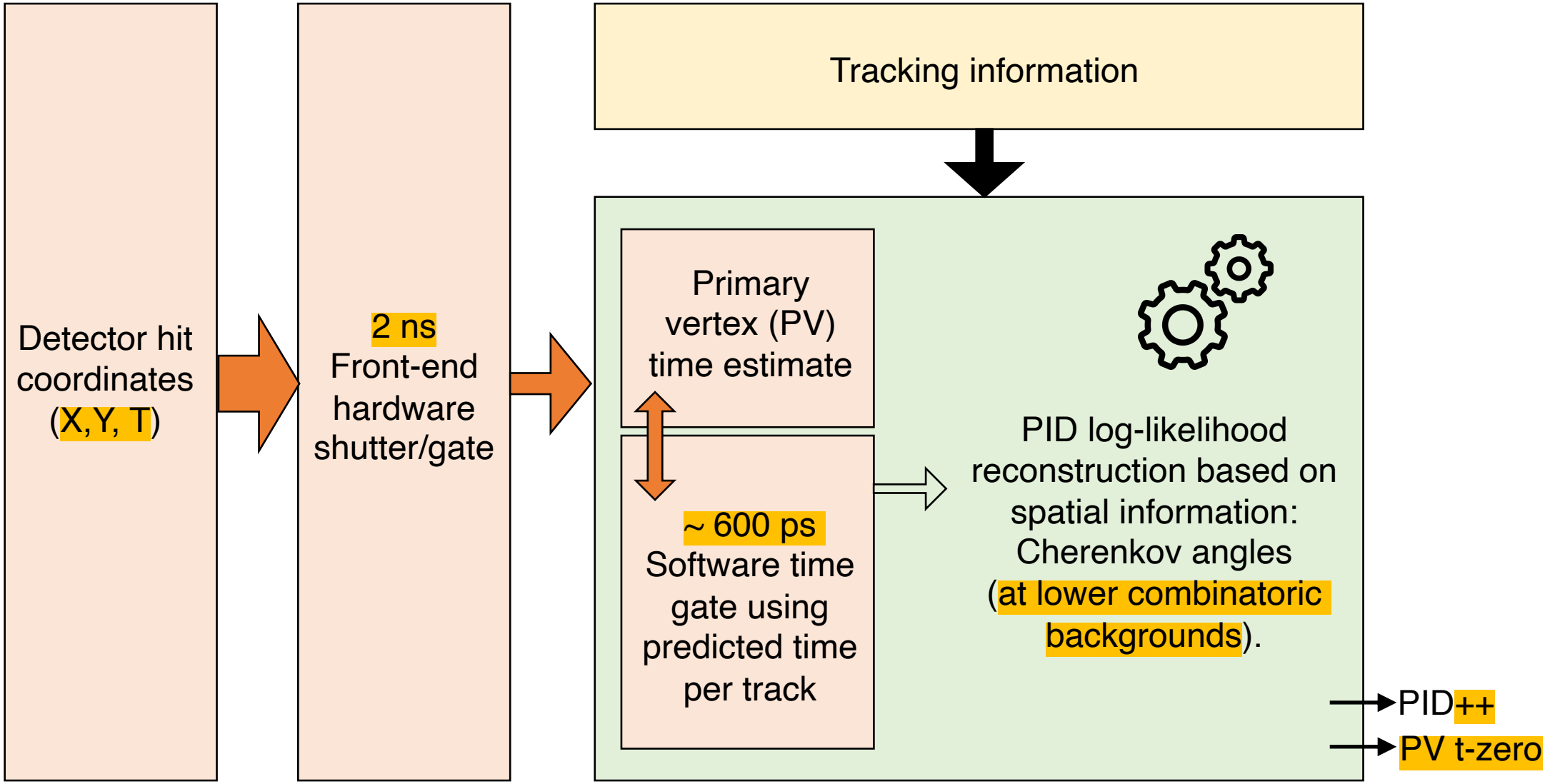
In practice, the performance is limited by the detector time resolution.

- The optimal software time gate is $\pm 2\ \sigma_{t,detector}$.
  (Narrower gates cut into signal and wider gates allow more background.)
- Run 4 MAPMTs have $\sigma_t \sim$ 150 ps resulting in a 600 ps optimal gate.
- Oversampling in the electronics allows suitable tuning of the gate width.

Run 3 front-end and reconstruction



Run 4 front-end and reconstruction



RICH estimate of primary vertex (PV) t-zero during Run 4

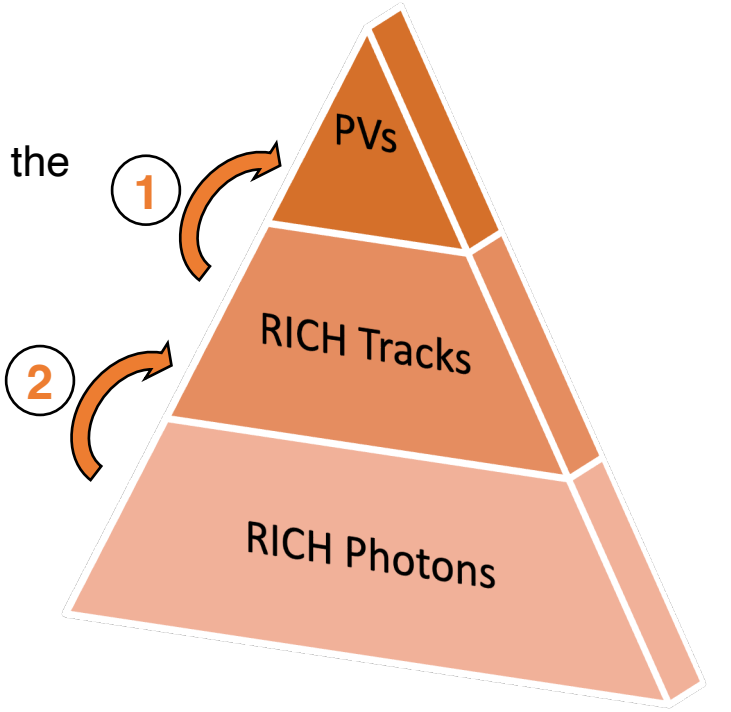
Using LS3 electronics enhancements, RICH can standalone estimate the PV t-zero.

- New measurement for the RICH detector and LHCb.

$$\langle t_0 \rangle_{PV} = \sum_{\text{true phot} \leftrightarrow \text{PV relations}} \left[t_{hit} - \frac{|\mathbf{r_A}|}{c} \sqrt{1 + \left(\frac{mc}{p}\right)^2} - \frac{d_{A,E}}{c} n \cos\theta_c - \left[d_{E,M1} + d_{M1,M2} + d_{M2,HIT} \right] \frac{n}{c} \right]$$

Main challenge is the correct association of photons to their PV.

- Oversampling in electronics of the multitude of photons per PV allows the relatively large MAPMT transit-time spread (σ~150 ps) to be fitted.
- Stage 1: Using LHCb tracking container for PV reconstruction.
- Stage 2: Cuts (first studies) or iterative (alternative, but more CPU) approach inside the RICH algorithms to reduce combinatorics in associating photons to tracks.



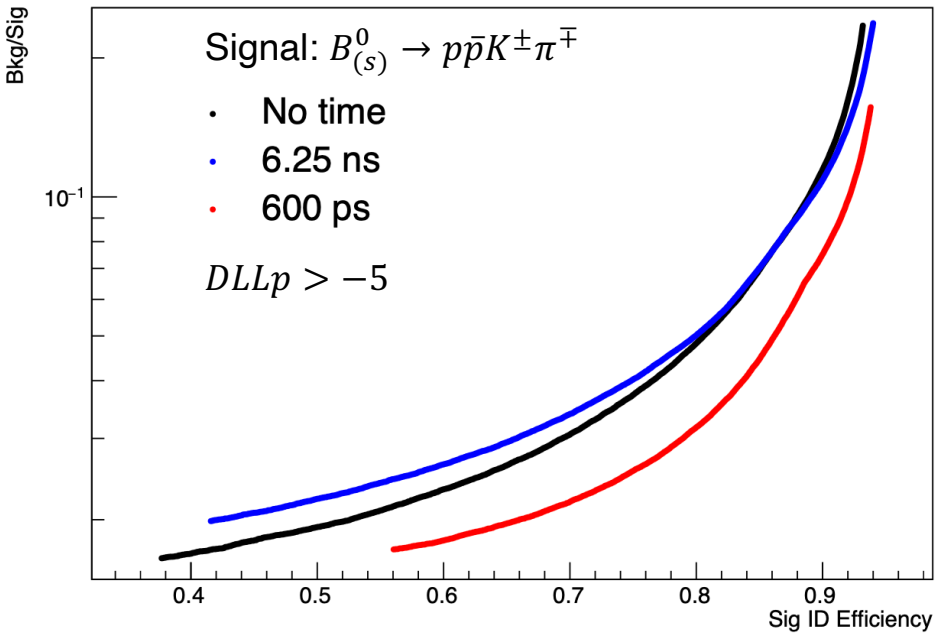
First (preliminary) studies showed a resolution better than 100 ps at least for a subset of PVs in the full LHCb simulation.

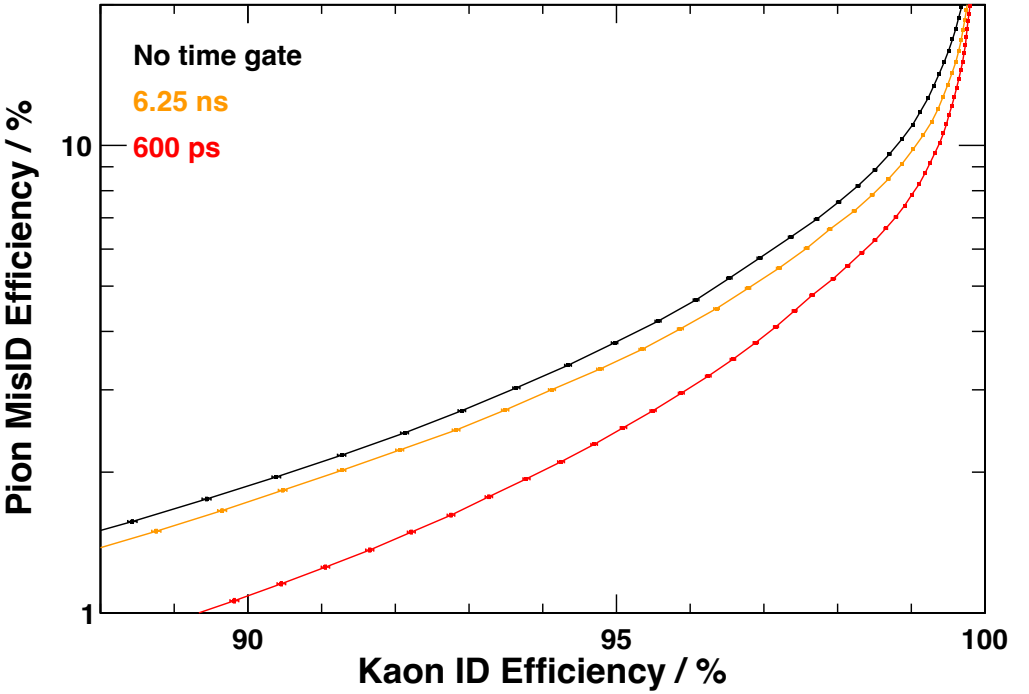
- Further software R&D foreseen.

Performance simulation for Run 4

Significant improvement in PID performance using the 600 ps Run 4 time gate.

- PV time from MC.
- MAPMT noise (dark counts, SIN) not included; purely photon backgrounds.
- Luminosity $\mathcal{L} = 3.0{\times}10^{33}\ \mathrm{cm}^{-2}\ \mathrm{s}^{-1}$ ($\nu = 11.4$), curves for Run 3 luminosity ($\nu = 7.6$) in backup.



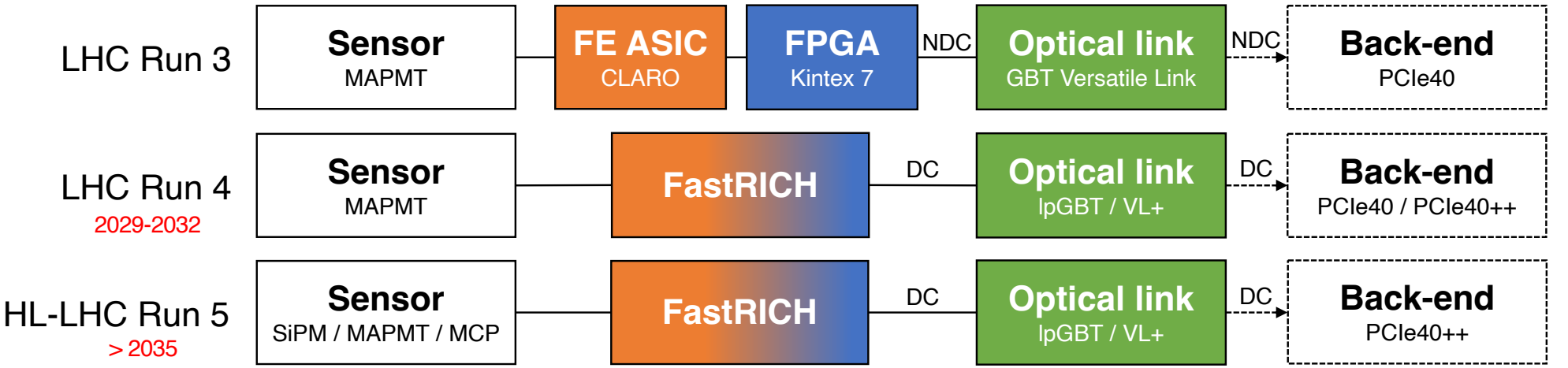


Effect on some physics channels using these Ntuples with 600 ps time gating was demonstrated in note LHCb-PUB-2021-009 with up to 70% background reduction.

- Recap: use of fast-timing information in Run 4.
- **New electronic readout chain.**
- FastRICH ASIC.
- Power and cooling of an elementary cell.

LS3 electronics chain

- Introduce the FastRICH ASIC.
- Change to data-compressed (DC) format at the front-end.
- Introduce the lpGBT/VL+ chipset.
- Modest expansion with PCIe40(0) at the back-end.



	Sensor	ASIC timewalk	FE time gate	TDC time bin
LHC Run 3	150 ps	< 4 ns	6.25 ns	None
LHC Run 4	150 ps	CFD correction	2 ns	25 ps
HL-LHC Run 5	~ 50 ps	CFD correction	2 ns	25 ps

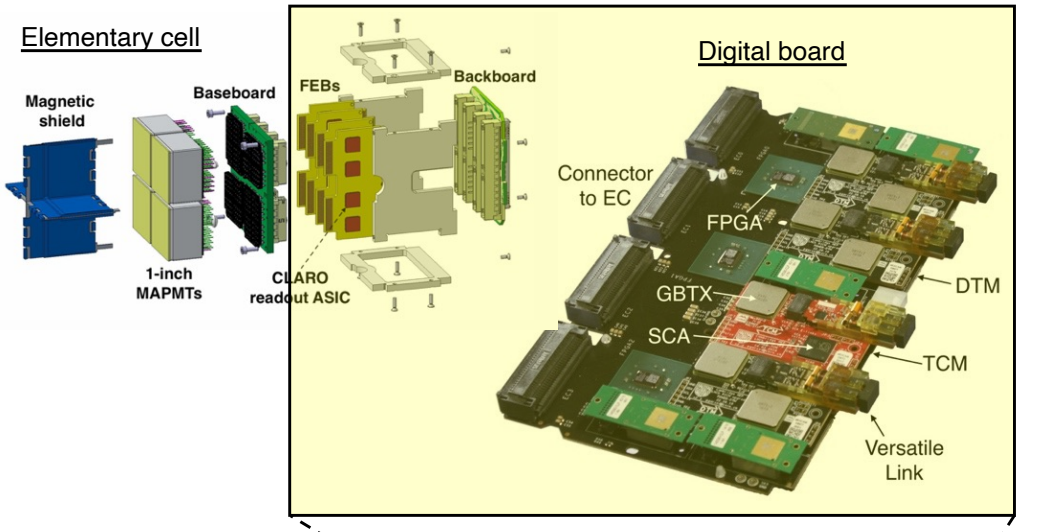
How is the Run 3 hardware affected?

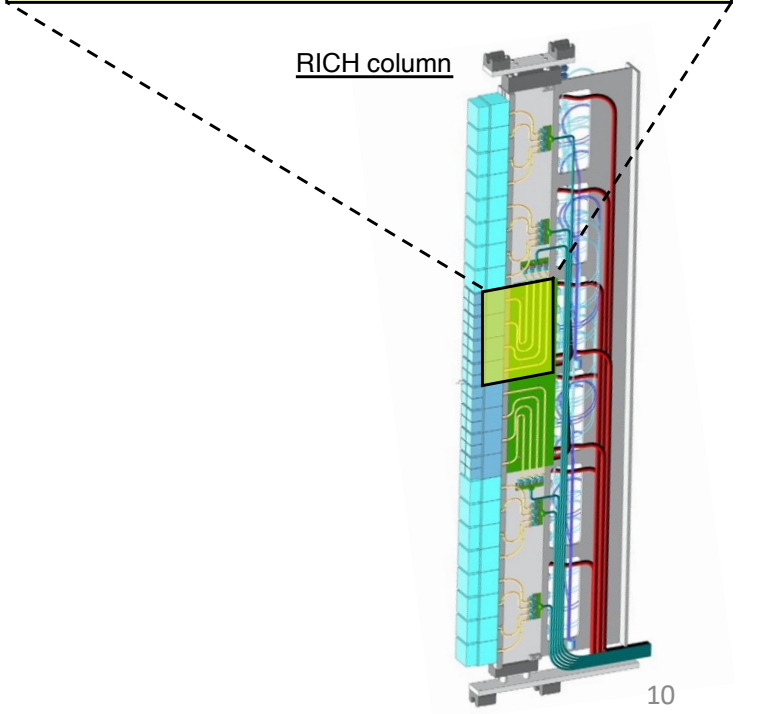
The LS3 programme is intended as an enhancement of the front-end readout only, keeping other services and components (cooling and power services, mechanics, optics and sensors) the same.

Remove:
- FEB with CLAROs.
- Digital boards (PDMDBs) with FPGAs.

Install:
- New boards with FastRICH.
- Adjustment to the elementary cell for cooling.
- New lpGBT/VTRX+ plug-ins.
- Additional PCIe40(0) cards for back-end processing.

Adjust:
- Fibre distribution to account for non-uniform occupancy.

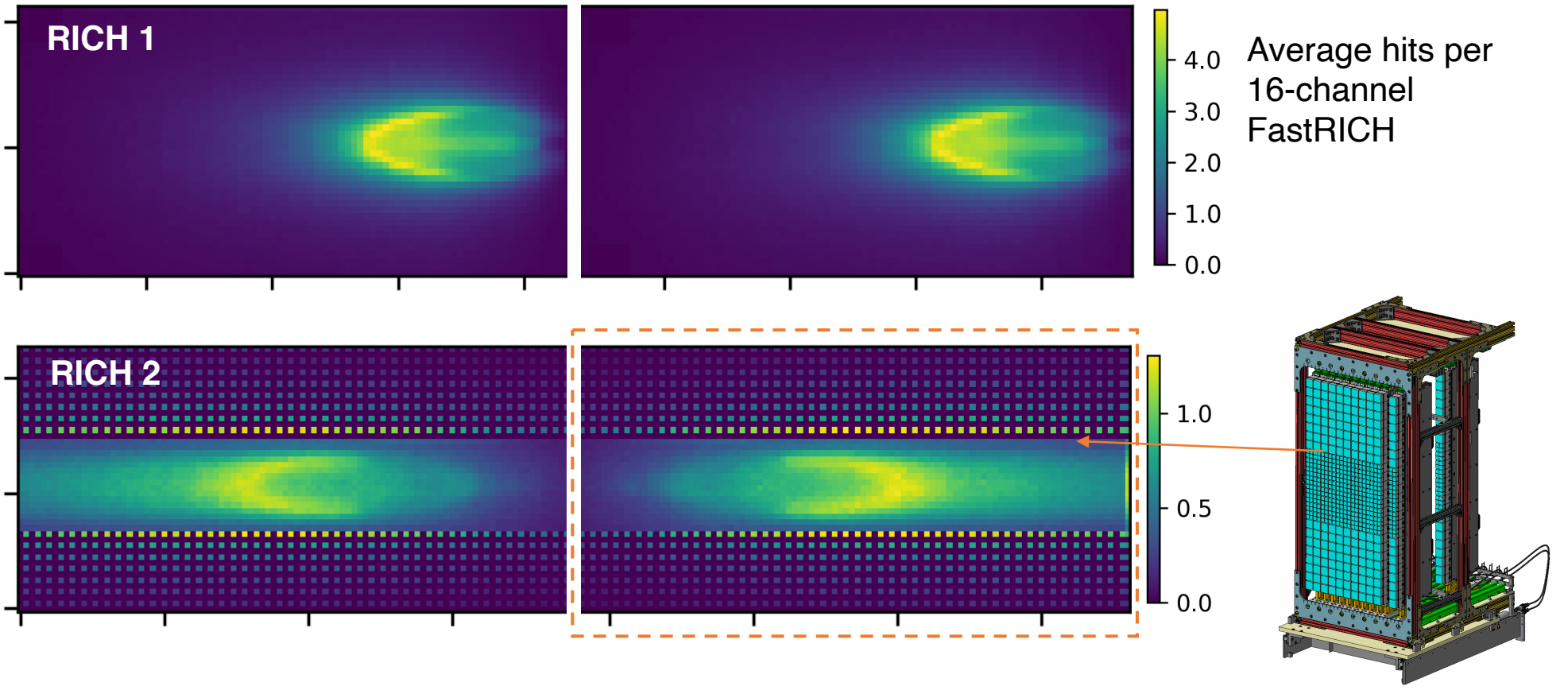




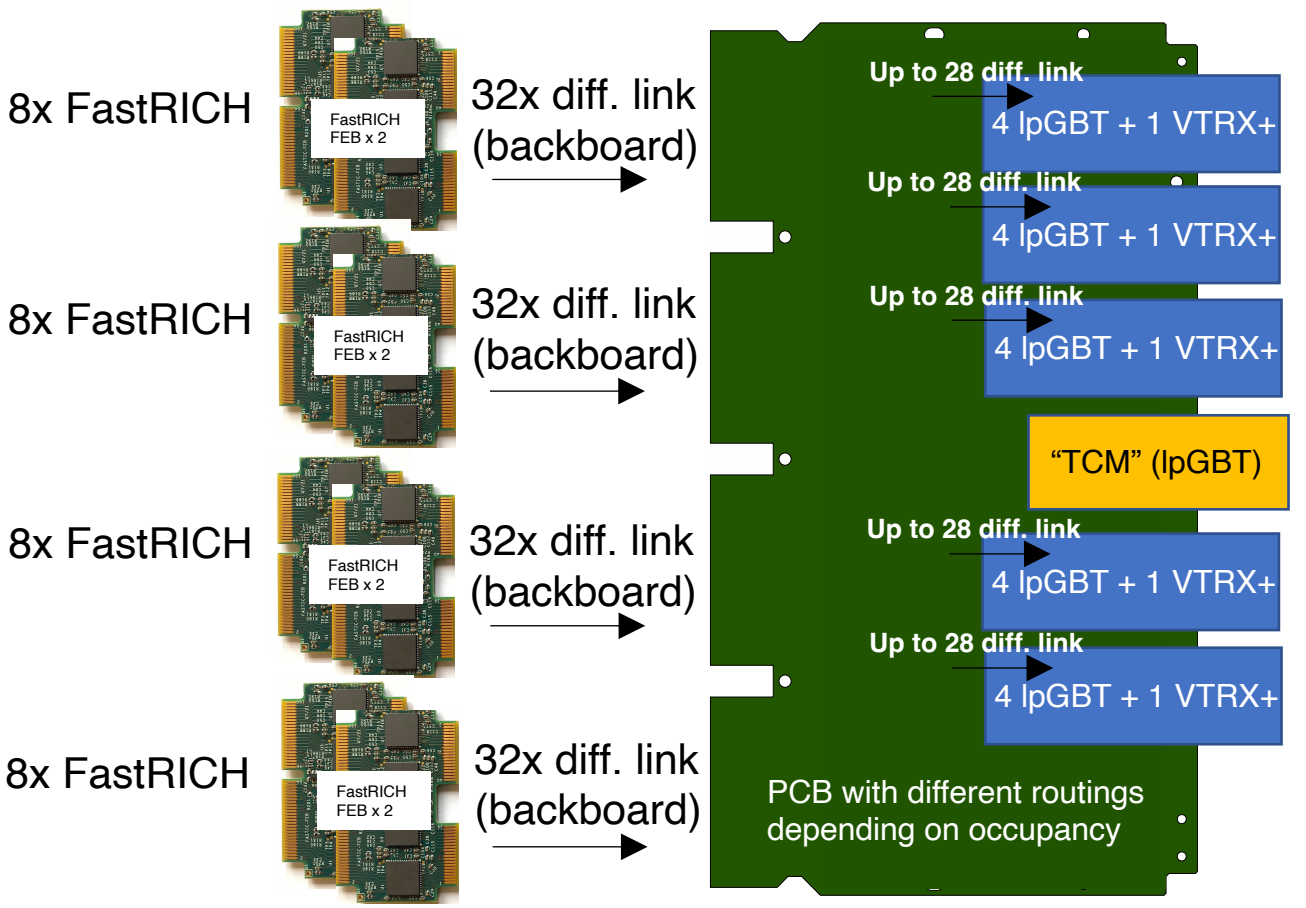
RICH hit maps: *highly non-uniform* photon occupancy

The non-uniform occupancy requires careful and non-uniform allocation of bandwidth resources across the detector. Most of the detector has < 1 hit per FastRICH per bunch-crossing *on average*.

- Strategy is to use data-compression in the FastRICH with configurable number (1, 2 or 4) of FastRICH output links and link speed (320, 640 or 1280 Mbps).



High-occupancy board (all FastRICH links enabled, 1280 Mbps)



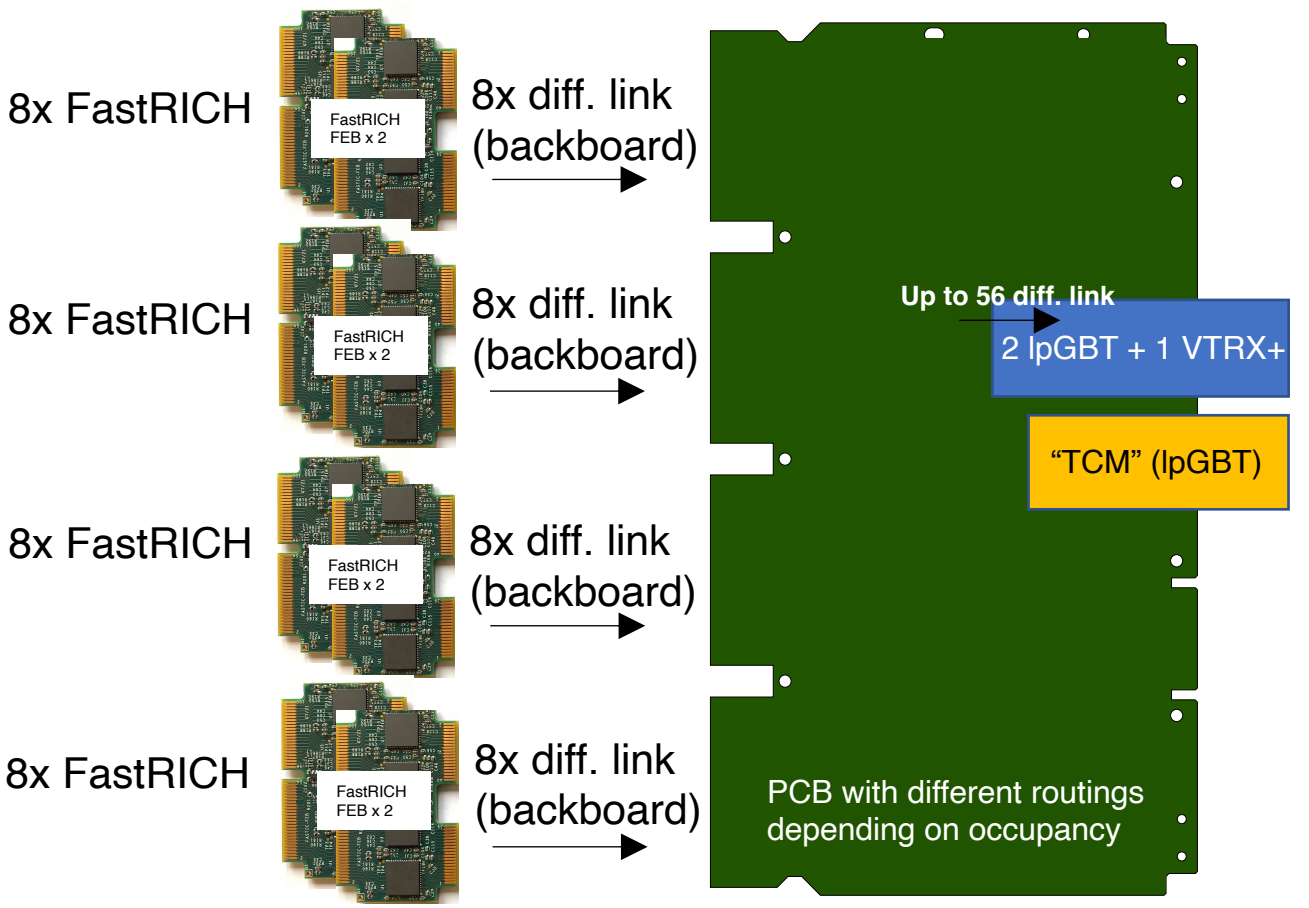
Preliminary and simplified sketch.

Motherboard (in green):
Passive PCB holding plug-ins for data transmission, controls and power regulation. Multiple versions of this card with different routing depending on occupancy.

Data transmission plug-in (in blue):
Single design @ 10 Gbps for the whole RICH, address non-uniformities using (a) number of plug-ins and (b) number of lpGBTs mounted per plug-in.
(Relatively complex design routing, may require high/low occupancy versions.)

Controls module (in yellow):
Distribution of clocks and fast & slow control commands to the FastRICHes.

Lowest-occupancy board (1 FastRICH link enabled, 320 Mbps)



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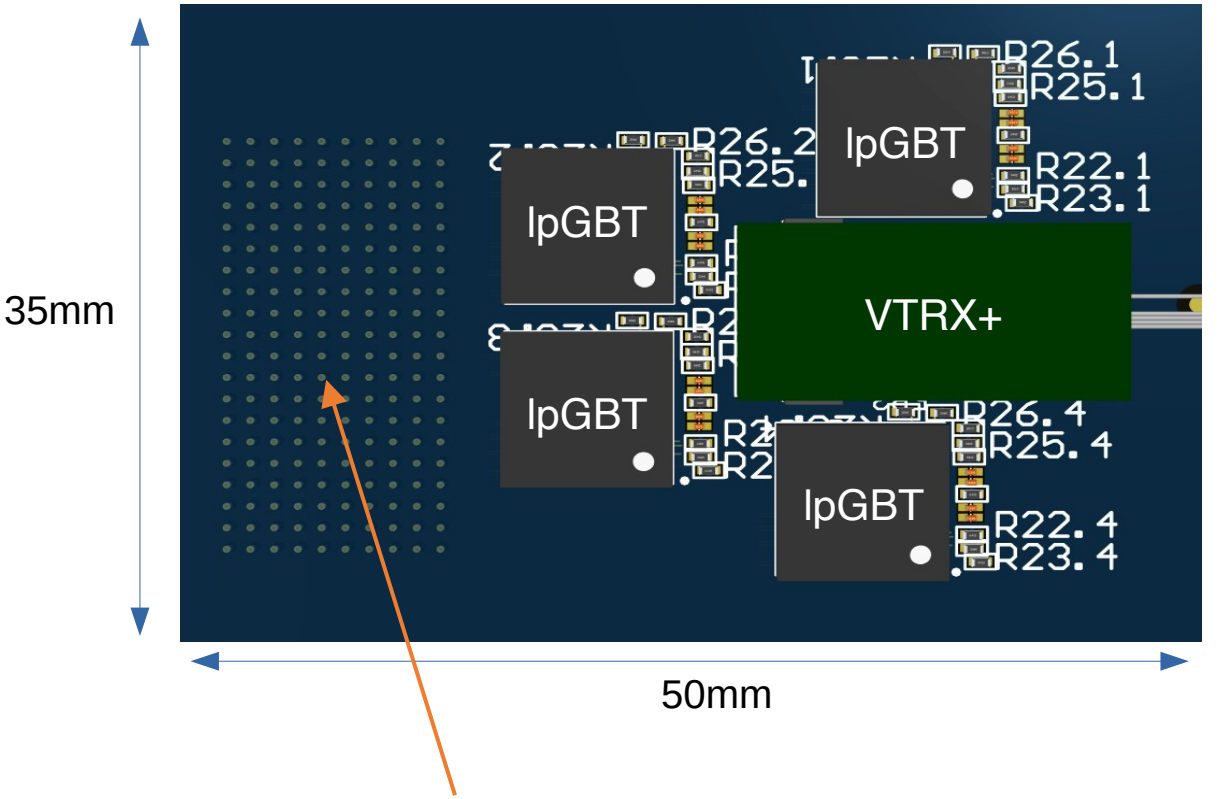
LpGBT plug-in prototype



Already under development for SPS beam tests this year:

- 3 TX lpGBT and 1 TxRx lpGBT
- coupled to 1 VTRX+.

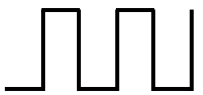
Allows 10 Gbps data transmission through compact ‘pig-tail’ fibre.

Coupled directly to the FastRICH ASIC through the digital motherboard.

LpGBT / VTRX+ chipset (and plug-in design) also foreseen to be used in Upgrade II.

Clock, configuration, control and monitoring interfaces

The lpGBT will be used for data transmission but also to distribute clock, control and monitoring signals.

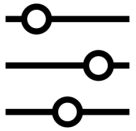


Clocks ultimately come from the master lpGBT downlink.

- Reference clocks required for lpGBT and FastRICH.
- Low jitter input clock and distribution important - to be evaluated with prototypes.
- May need multi-drop clock network.

Fast synchronous signals are required for LHCb operation.

- E.g. BCR, ECR, SYNC, Test Pulse.
- Expect minimal impact on SOL40 operation (even some simplification may be possible).



Configuration commands, possibly through the master lpGBT I2C interface (3 available).

- FastRICH ASIC and TX lpGBT configuration required.

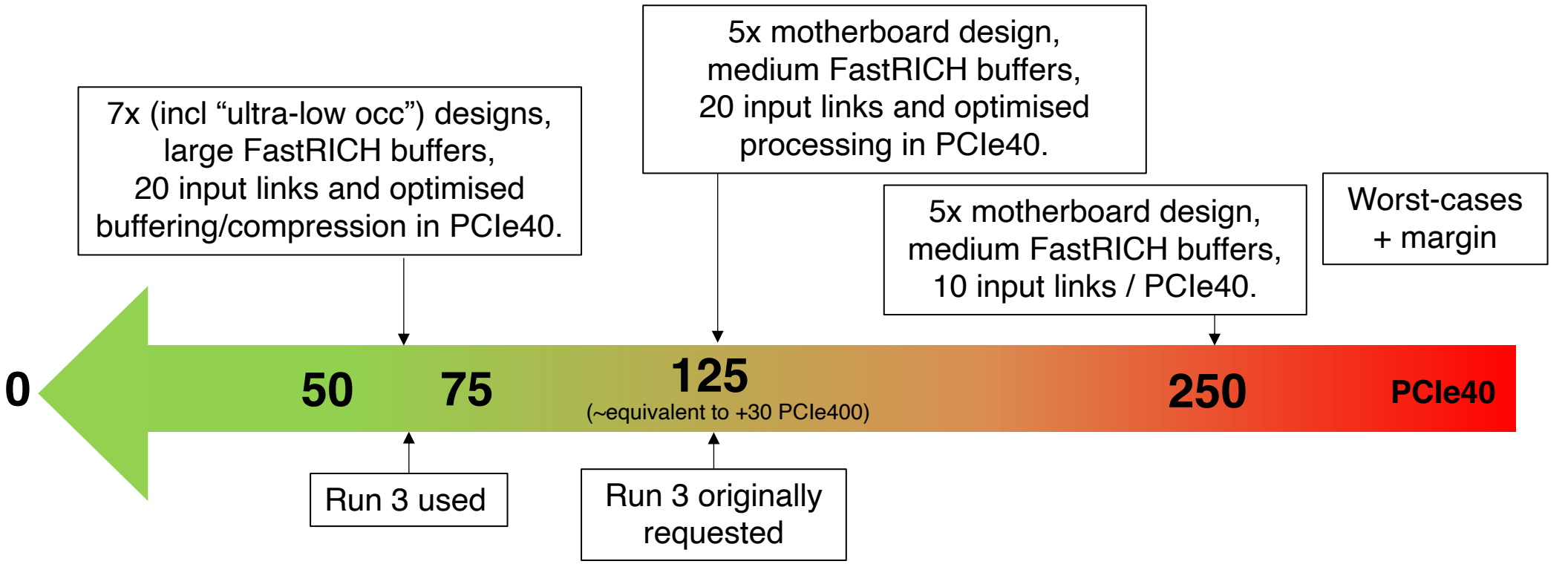
Monitoring interfaces will be kept similar to Run 3.

- Thermistors for temperature.
- Voltage and SEL (single-event upset) monitoring.

Preliminary bandwidth simulation studies

Estimated the required bandwidth capacity to account for fluctuations in 4000 simulated LHCb bunch crossings for the Run 3 detector + FastRICH data format and a user-defined ASIC event buffer size.

- Configuring the lpGBTs to 10 Gbps and adding some uniform Poisson background of 5% in RICH1 and 2% in RICH2 across the full plane.
- Estimated ~2500 lpGBTs and a link capacity of ~20 Tbps, while the data throughput is less than that.
- Next steps will include header data and more detailed digital board modularities.



- Recap: use of fast-timing information in Run 4.
- New electronic readout chain.
- **FastRICH ASIC.**
- Power and cooling of an elementary cell.

FastRICH specifications

A highly-expert team at CERN-EP-ESE and the University of Barcelona is developing the FastRICH ASIC with strong input from the RICH group.

The ASIC is tailored for high flexibility and compatible with MAPMTs (LS3 enhancements) and Upgrade II photon sensors.

Time resolution: TDC with ~ 25 ps time bins.

Power consumption: ~ 8 mW per channel in 16-channel ASIC.

LHCb compatibility: direct coupling to lpGBT, radiation hardness for ~ 10^{13} n_{eq}/cm^2 and ~ 5 kGy and > 40 MHz readout rate.

Appendix A: FastRICH specifications

Table 2: Preliminary specifications for the FastRICH ASIC for the LHCb RICH LS3 enhancements and Upgrade II.

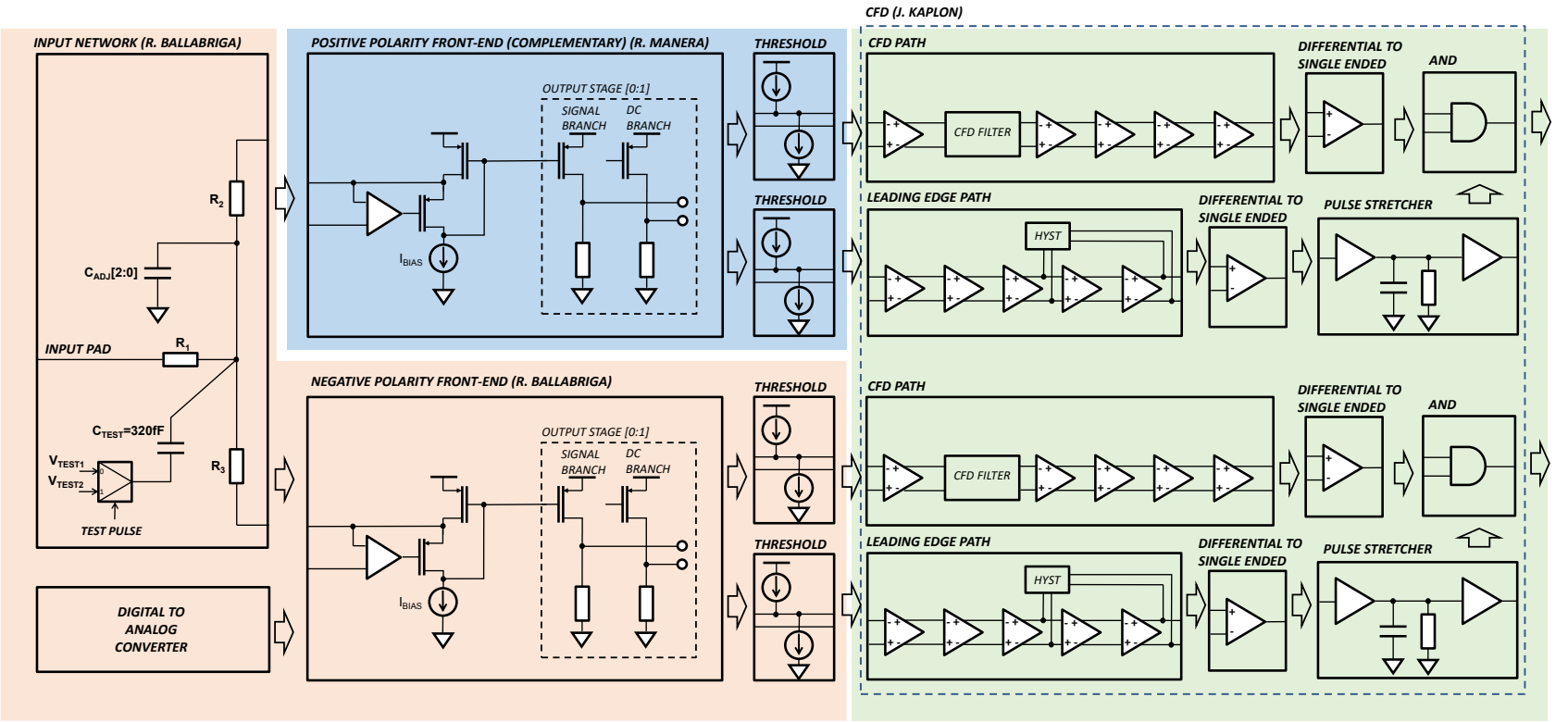
Parameter	Specification
Technology	65 nm CMOS
Die dimensions / # of pads	$3 \times 4\,mm^2$ / $\mathcal{O}(100)^2$
Package / sensor coupling	BGA with pitch ≥ 0.8 mm
Radiation hardness	Yes (TID > 100 Mrad and triplication)
# of channels	16
Channel type	Linear (i.e. not pixelated)
Channel connection	Single-ended
Polarity	Configurable positive or negative
Input signal attenuation	Configurable per channel: 1, 1/2, 1/4, 1/8
TDC time bin	25 ps
Electronics time jitter	~ 30 ps RMS SPTR
Residual time walk	< 200 ps pk-to-pk (after CFD, over 50 μA to 5 mA range)
Time gate	2 ns nominal, configurable width and offset to the 40 MHz clock
Power consumption analog	Target < 4 mW *
Power consumption digital	~ 2 mW per channel
Energy resolution	Non linear (not required when CFD is implemented). Possibility of an additional threshold level, increasing the output bandwidth by 1 bit/hit
Dynamic range	5 μA to 5 mA **
Maximum front-end rate	> 50 MHz (non-linear ToT mode. Sensor dependent)
Testing and calibration	Internal test charge generation controlled by digital signal
Slow control interface	I2C with multiple chips on the same I2C bus
VCO oscillation freq.	1.66 GHz
# of VCO stages	12
Bits/event (ToA)	fToA @500ps: 2 (Assumes a 2 ns gate) ufToA @20ps: 5
Total bits/event	7 ToA (2 fToA, 5 ufToA) 4 Channel identification 1 Threshold high hit (only Upgrade II)
Output	Digital differential, lpGBT compatible
Output links freq.	160, 320, 640, 1280 MHz
# of output links	Programmable at chip level to 1, 2 or 4

* Including CFD and a branch for second ('2 bit') threshold level.

** While 5 μA can be reached in terms of electronic noise, the timing performance can be achieved over the range 50 μA to 5 mA.

FastRICH analogue front-end design

- Input network with high dynamic range: 50 μA to few mA for MAPMT, SiPM or MCP coupling.
- Test pulse DAC for testing purposes.
- Positive or negative polarity signal processing.
- Novel Constant-Fraction Discrimination (CFD) to reduce throughput (no ToT information).
- Optional leading-edge path without recovery time (~15 ns for CFD).
- Logic blocks can be switched on/off for optimal power consumption.



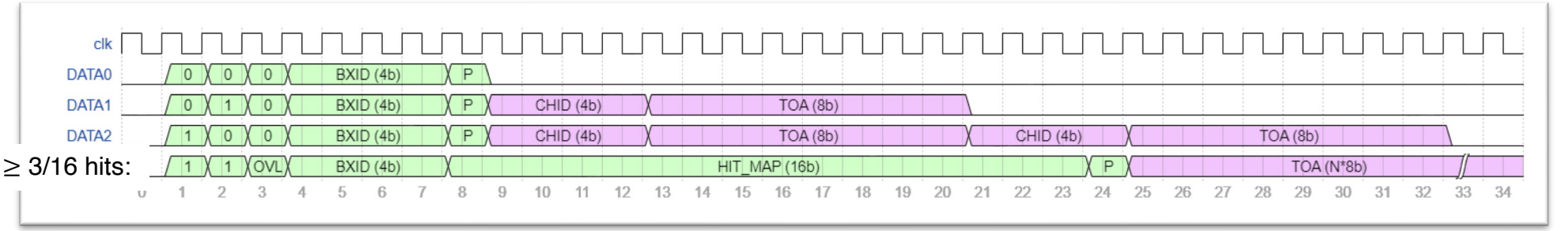
FastRICH digital front-end design

Front-end hardware time gate of configurable width / offset (2 ns nominal) to reduce data throughput.

Configurable number and speed of output links allows optimisation of data link resources.

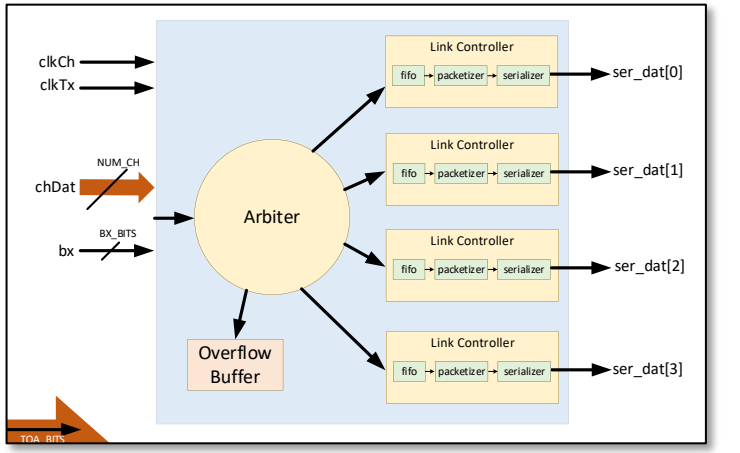
Preliminary zero-suppression scheme has been defined:

- Format that depends on the occupancy gives best performance.
- Implementation, additional headers and compatibility with the LHCb framework are work-in-progress.



An arbiter sends buffered events on the next-available eLink.

- "Vertical buffering" optimises front-end and lpGBT usage.
- Introduces a per-link latency at the back-end, specifications on the maximum allowed latency are under study.



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Front-end power consumption and distribution

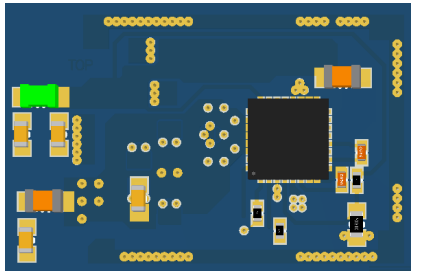
(Watts)	ASIC	FPGA	Master	TX	Total
Run 3	1	4.5	2	7	14.5
Run 4	4	-	0.5	≤ 7	11.5

Per ½ PDM excluding DCDC contributions.

Initial estimates are that the total LV power consumption will decrease.

- However, the power consumption is more concentrated in the elementary cell (EC).
- Requires improved EC thermal coupling to cold bar (next slide).
- LS3 enhancements reset irradiation damage.

Maraton 7V



LpGBT plug-ins	2(3) bPOL12V @ 1.2V 1 bPOL12V @ 2.5V
FastRICH	1(2) bPOL12V @ 1.2V

Foresee to use bPOL12V regulators on the digital motherboard.

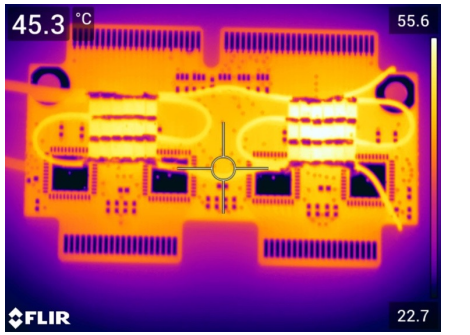
- Maraton 7V power infrastructure remains unchanged for LS3 and may even be operated at lower voltage (under study).

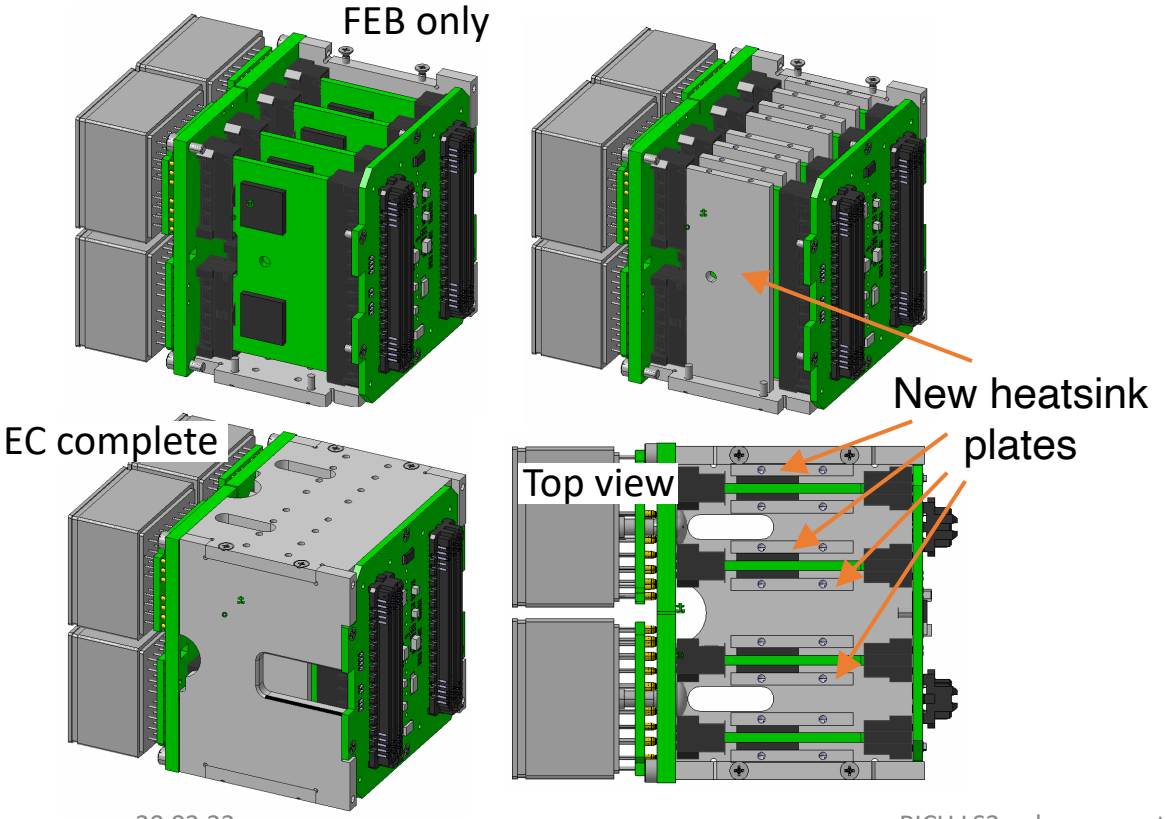
Improved EC for FastRICH coupling to (cold) column

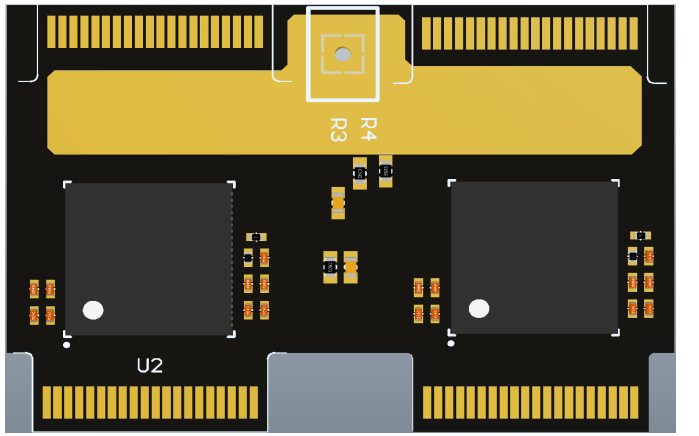
Increased power in the EC needs to be removed through the column to avoid warming up the sensors.

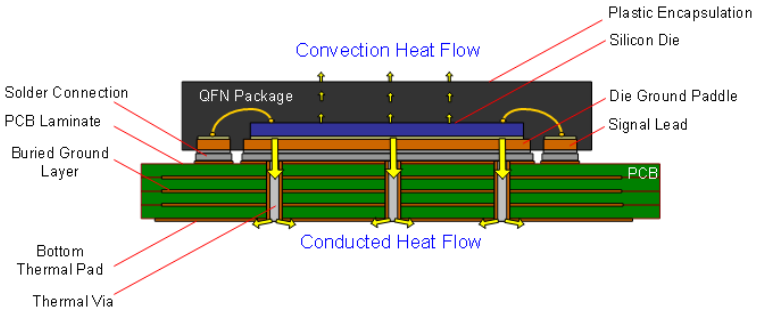
Detailed studies ongoing investigating two solutions or a combination thereof:

- Introduce heatsink plates with thermal contact to the FastRICH package.
- Design the FEB with large copper area to provide a thermal path between the FastRICH and column through the backboard.









Conclusion

RICH LS3 enhancements aim to equip the detector with new front-end readout electronics including the FastRICH ASIC capable of timestamping photon detector hits with ~25 ps time bins, thereby:

- Adding the time dimension to the RICH and LHCb (PV timestamp),
- Improving PID during Run 4,
- Preparing for Upgrade II with fast-timing electronics coupled to new photon sensors and
- Profit optimally from the 3-year maintenance period during LS3.

The novel FastRICH ASIC will include data-compression features (CFD, time gate, zero-suppression) and will be compatible with the lpGBT / VTRX+ optical link chipset and LHCb protocols.

The detector will be designed for non-uniform data throughput. Most of the detector (cooling and power services, mechanics, optics and sensors) will be kept unchanged.

Backup

RICH photon time-of-arrival is highly predictable

Using the RICH reconstruction algorithms, for a given primary vertex (PV) start time, it can be accurately predicted when a photon is expected to arrive.

➢ For this we use the reconstructed track and photon path.

Track path length to the RICH detector

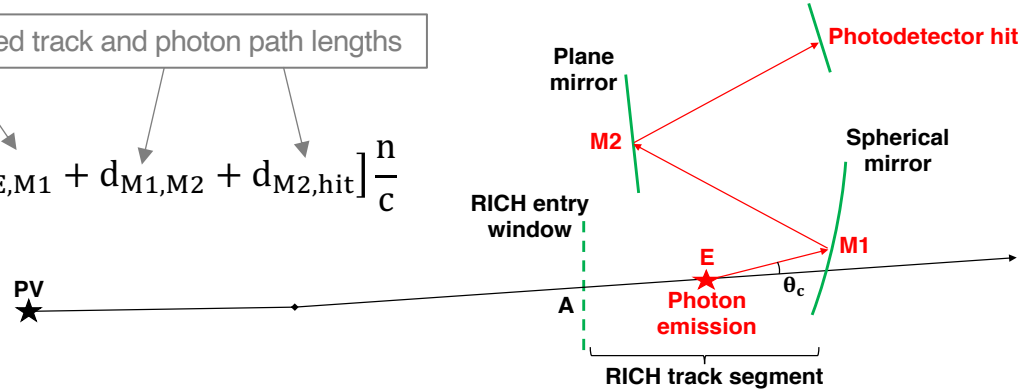
Mass hypothesis in RICH reconstruction

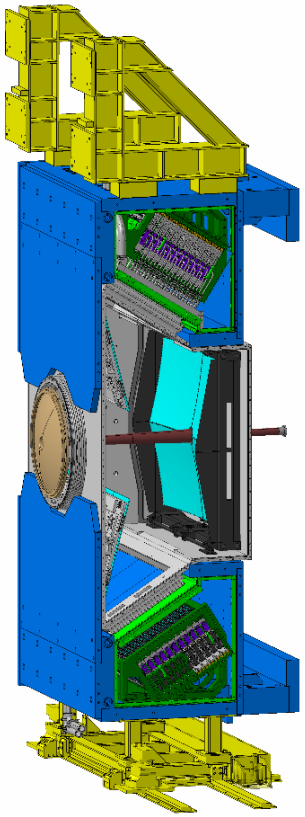
Reconstructed track and photon path lengths

$$t_{pred} = t_{pv} + \frac{d_{pv,A}}{c}\sqrt{1+\left(\frac{mc}{p}\right)^2} + \frac{d_{A,E}}{c}\, n\cos\theta_c + \left[d_{E,M1} + d_{M1,M2} + d_{M2,hit}\right]\frac{n}{c}$$

Primary vertex time

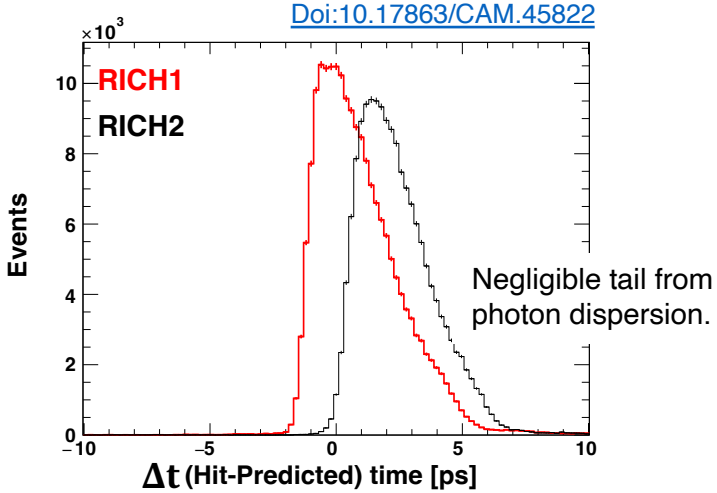
Momentum from LHCb tracking





+ RICH 2 path length correction for curved tracks.

Doi:10.17863/CAM.45822



Taking all contributions into account (+ PV time from MC), obtain a prediction of better than 10 ps.

➢ For photon detectors 'the faster the better', as in practice this time resolution will dominate the performance.

Additional PID curves at Run 3 luminosity

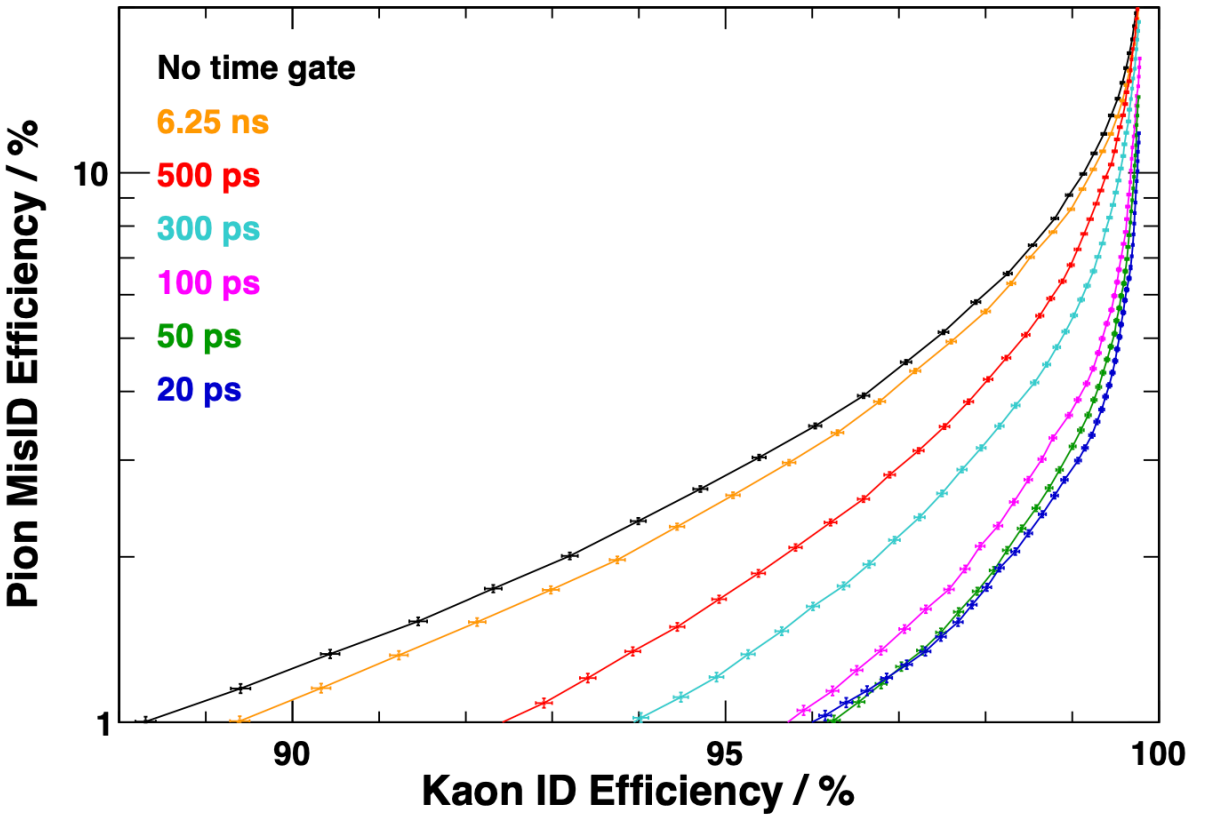
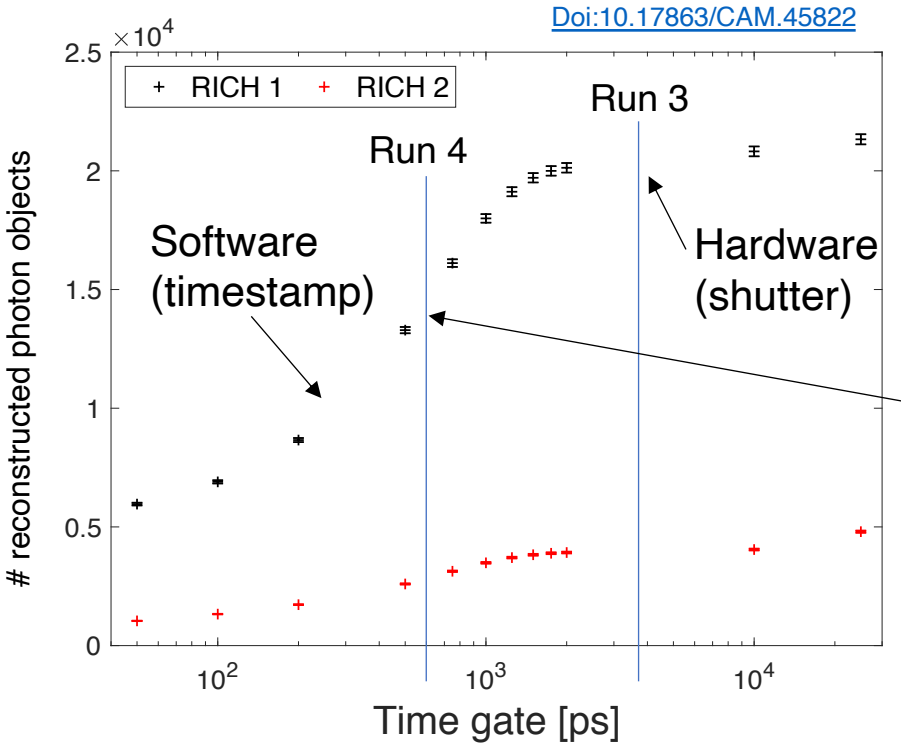
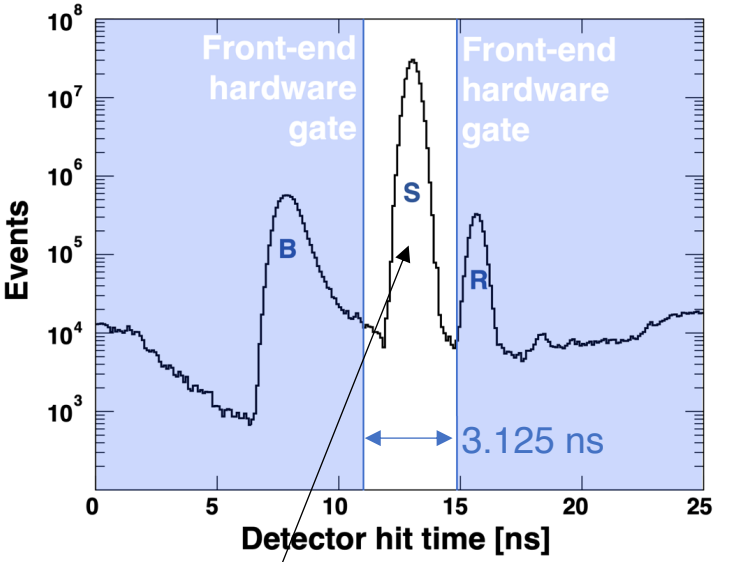


Figure 3: PID curves at $\mathcal{L} = 2.0 \times 10^{33}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ and 'ideal' photon detector time resolution, for software time gates ranging from 25 ns to 20 ps.

Time gate in the reconstruction software





The Run 4 software time gate will reduce the number of combinations of tracks <-> photons (“photon objects”) in the reconstruction algorithm.

“Resolving the signal peak” leads to improvements in PID (and potentially computing power at the log-likelihood).

FastRICH timeline

	2021			2022				2023				2024			
	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
TDC Ring oscillator															
PLL															
Constant Fraction Discriminator Study															
Project start															
Architectural definition, definition interface															
Analog design															
Analog verification															
Digital design															
Chip integration and verification															
ASIC submission															
Test setup preparation															
Electrical testing, radiation tests, test beams															
Redesign (if required)															
Verification (if required)															
ASIC resubmission (if required)															

- Analogue design currently in completion and verification ongoing.
- Digital design advancing rapidly. Here, the PLL / TDC circuit blocks strongly benefit from synergies with the FastIC+ development (targeting in particular medical applications).

PCIe40(0) / online infrastructure in the cavern

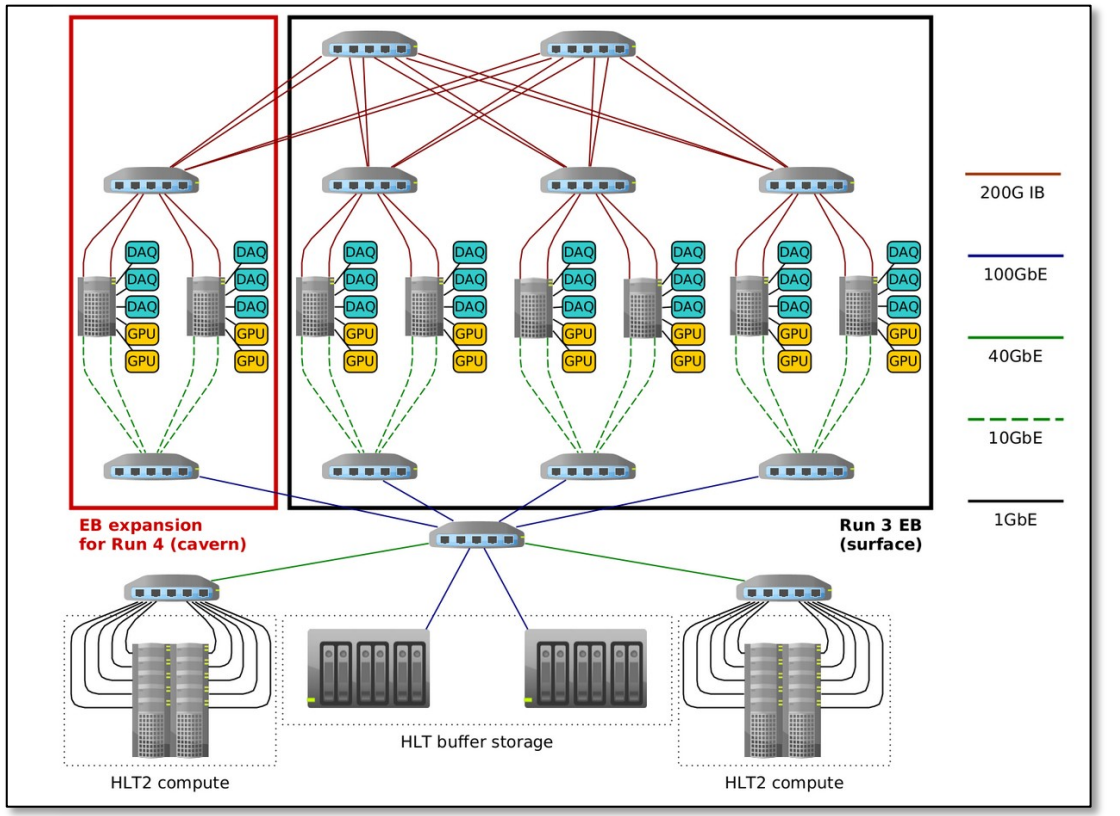
New infrastructure will be installed in the cavern during LS3.

- New shorter fibres capable of 10 Gbps.
- Funds are reserved for a modest expansion of the back-end PCIe40(0) resources.
- We're highly motivated to employ PCIe400s, looking forward also to Upgrade II.

The ZS data format will require additional processing for unpacking and decoding at the back-end. Developments in this decoding need to closely follow the FastRICH data format definition, which is currently WIP together with the ASIC team.

- Need to evaluate the implications of vertical buffering and back-end latency between links with the help of online experts.

Tommaso Colombo (electronics workshop)



Quality Assurance draft schedule

Proposed modification to existing RICH detector columns can start after the beginning of LS3.

- Programme largely based at CERN for assembly and test of new ECs in supervised area.

Important milestones are receipt of the FastRICH ASIC and the commissioning of the first column.

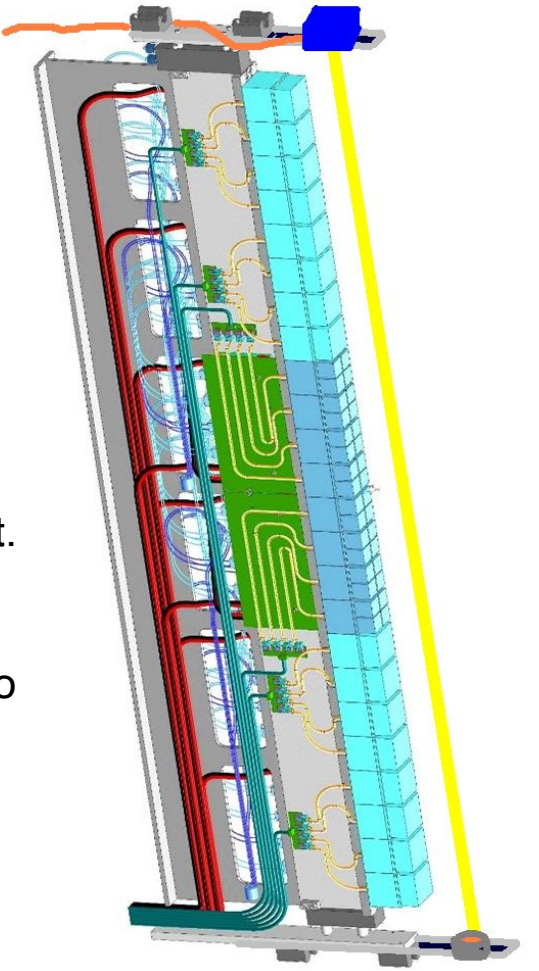
Preliminary schedule accounts for 9 months of commissioning during LS3 after installation in the cavern, in order to be ready for the 2029 physics production year for LHCb.

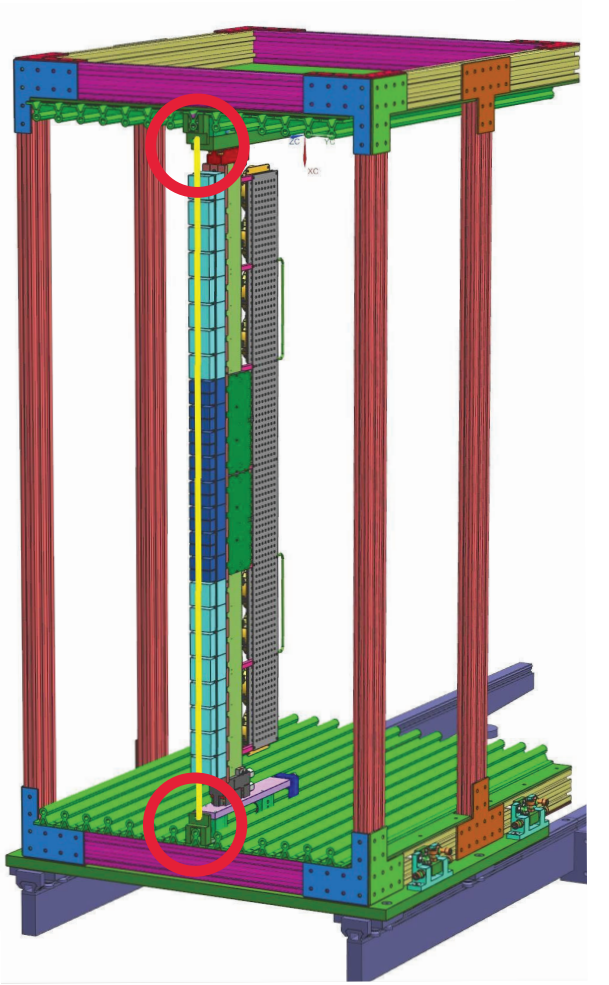
Preparation	2025				2026				2027				2028				2029 - 2032			
Execution	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
FastRICH QA																				
FEB QA																				
Backboard QA																				
EC+ mounting (QA)																				
Digital Boards QA																				
Columns dismantling																				
Columns assembly																				
Columns commissioning																				
Installation																				
Commissioning at P8																				
Operations																				

Column calibration and monitoring system

Proposed new technique for column testing, calibration and monitoring based on a Rayleigh scattered laser beam.

- Online measurement of absolute/relative gain/efficiency and tool to perform precise time alignment.
- Method being investigated in the lab to assess the uniformity and timing.
- Once validated in the lab, possibility to use this technique not only in the full detector but also during column commissioning.

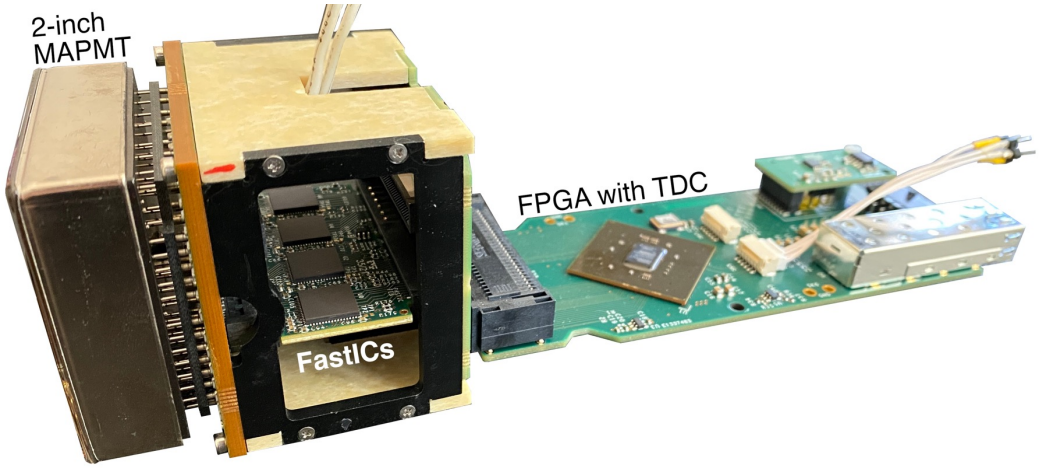


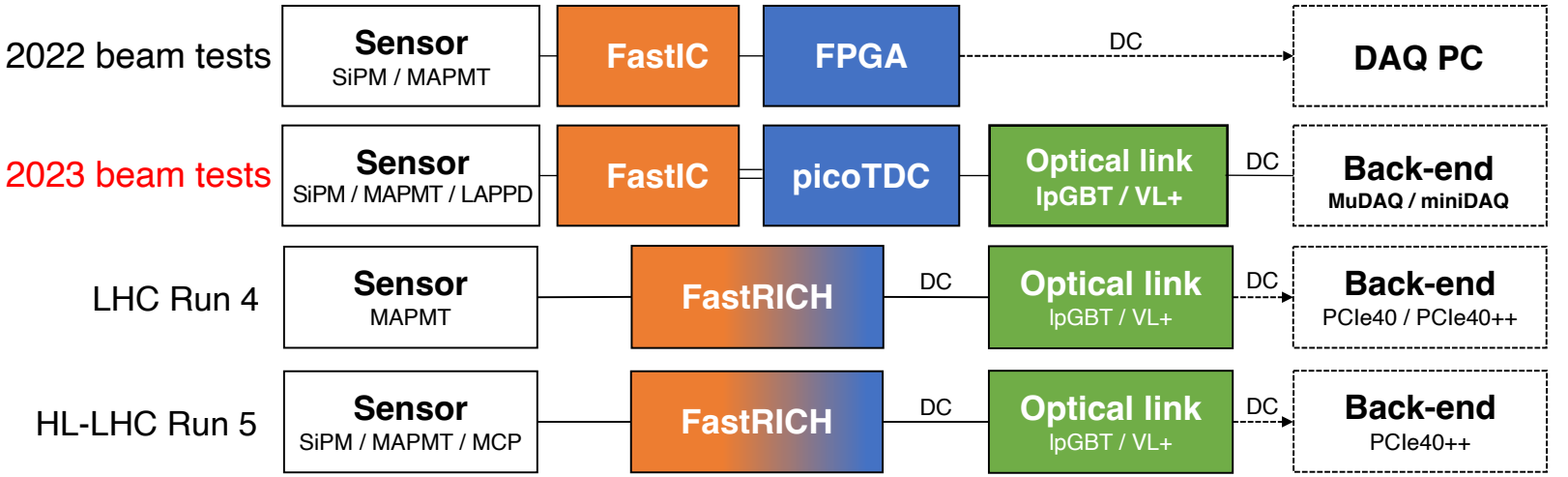


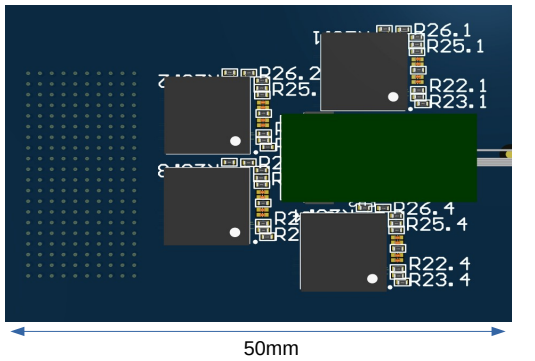
SPS beam tests of prototype fast-timing chain

The test beam campaign focuses on the development and testing of prototype readout chains with fast-timing information. The FastIC under study will be the predecessor of the FastRICH for LS3.

- FastIC was coupled to SiPMs and MAPMTs.
- Readout electronics are evolving to introduce the lpGBT/VTRX+ in 2023 and to be optimally setup to integrate and test the prototype FastRICH ASIC from 2024 onwards.







SPS beam tests of prototype fast-timing chain

Valuable information was collected on fast-timing techniques, FastIC operation, sensor coupling, clock and signal distribution etc.

Superimposed hit maps show detected arcs from the Cherenkov ring (orange-dotted line) during beam tests.

Analyses of timing performance are ongoing with preliminary best estimate of ~ 230 ps SPTR for MAPMTs (approaching the 150 ps TTS), with scope for further improvements in the analyses, track reference timestamp, etc.