PicoCal Electronics

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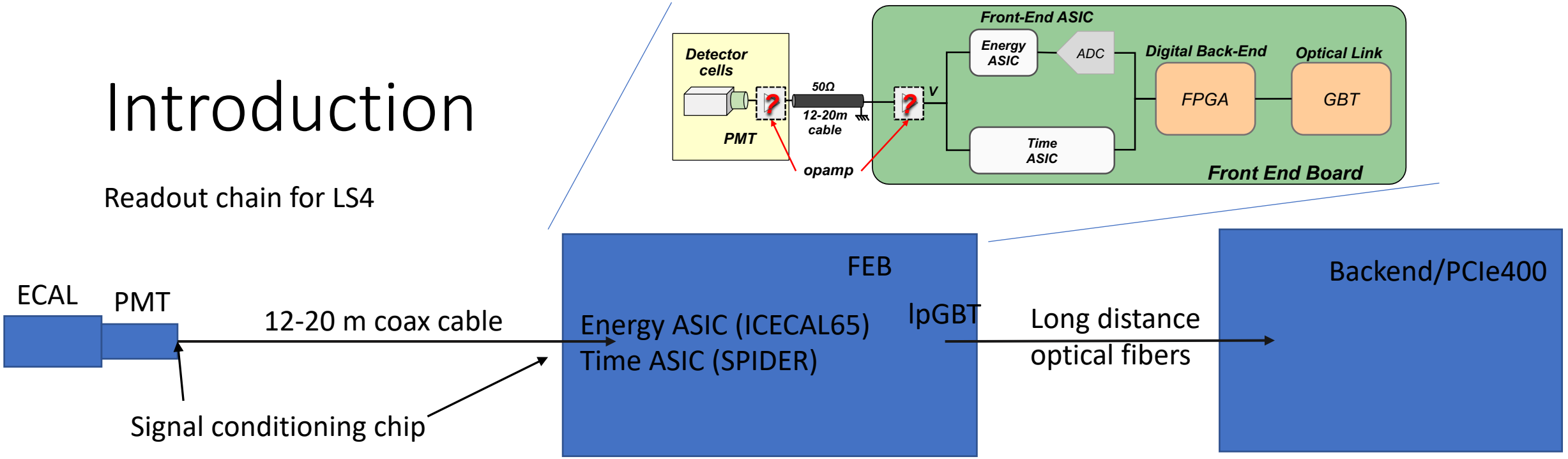
Introduction

Readout chain for LS4



- Requirements for electronics for LS4:
  - Energy measurement on 12 bits, on a large dynamic range, E_T=0 to O(100 GeV)
  - Time measurement with 15ps rms resolution at large energies (E_T~1 GeV), for the entire chain (Detector, PMT, cable and electronics)
  - FEBs located on the ECAL platform: modest radiation environment (~40 kRad)
  - Keep flexibility to include a timing layer in the readout, re-using most of the chain
  - Perform data reduction or pre-processing in the electronics when possible

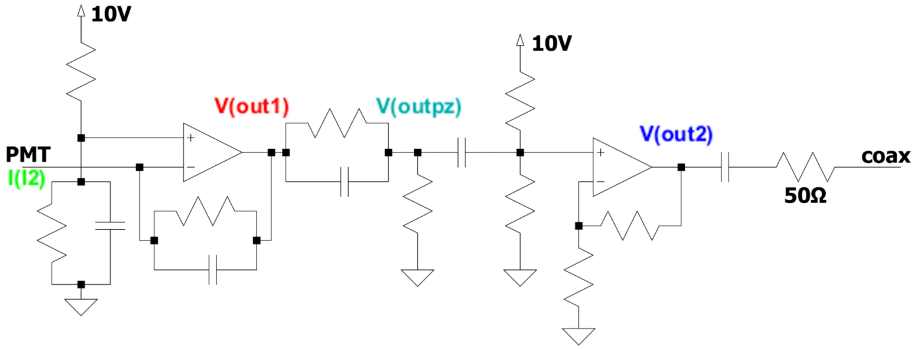
Run 3 electronics

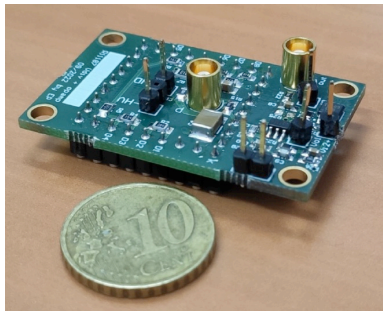
- No time measurement, smaller dynamic range (E_T = 0 to 20 GeV)
- 6016 channels, 32 channels per board: 188 boards in 14 crates
- No data processing (in FEB or PCIe40), all data sent offline: 12 bit ADC per channel + 40 bits LLT per board
- Institutes:
  - ICECAL ASIC: Barcelona/Valencia
  - FEB: IJCLab Orsay
  - PCIe40 firmware: LAPP Annecy

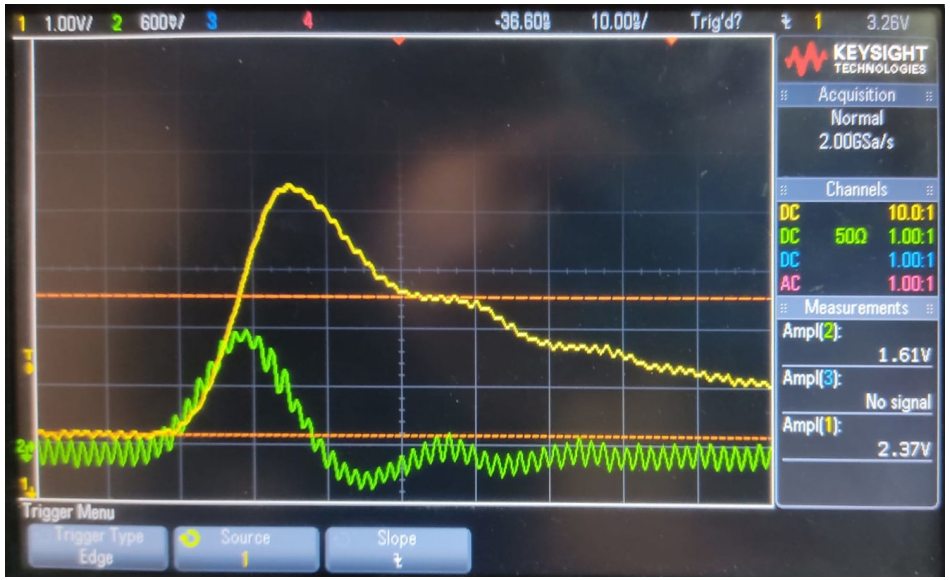
Barcelona/Valencia

COTS PMT conditioning circuit

- COTS based signal conditioning circuit, placed either at the base of the PMT (if radiation hardness allows) or at the input of the FEB, to compensate signal losses in the coaxial cable
- Goal: deliver voltage signal with range of ~2V to facilitate signal distribution to each path (E/t)
- First prototype produced and tested
  - Source AWG with GFAG signal shape
  - Pole Zero cancellation reduces the signal width
  - Amplification modified during tests
  - Stability has to be reviewed
- Second version under design
  - Market search for different options of op-amps
  - Flexible design for interchangeable op-amps
  - Aiming for test beam evaluation this year

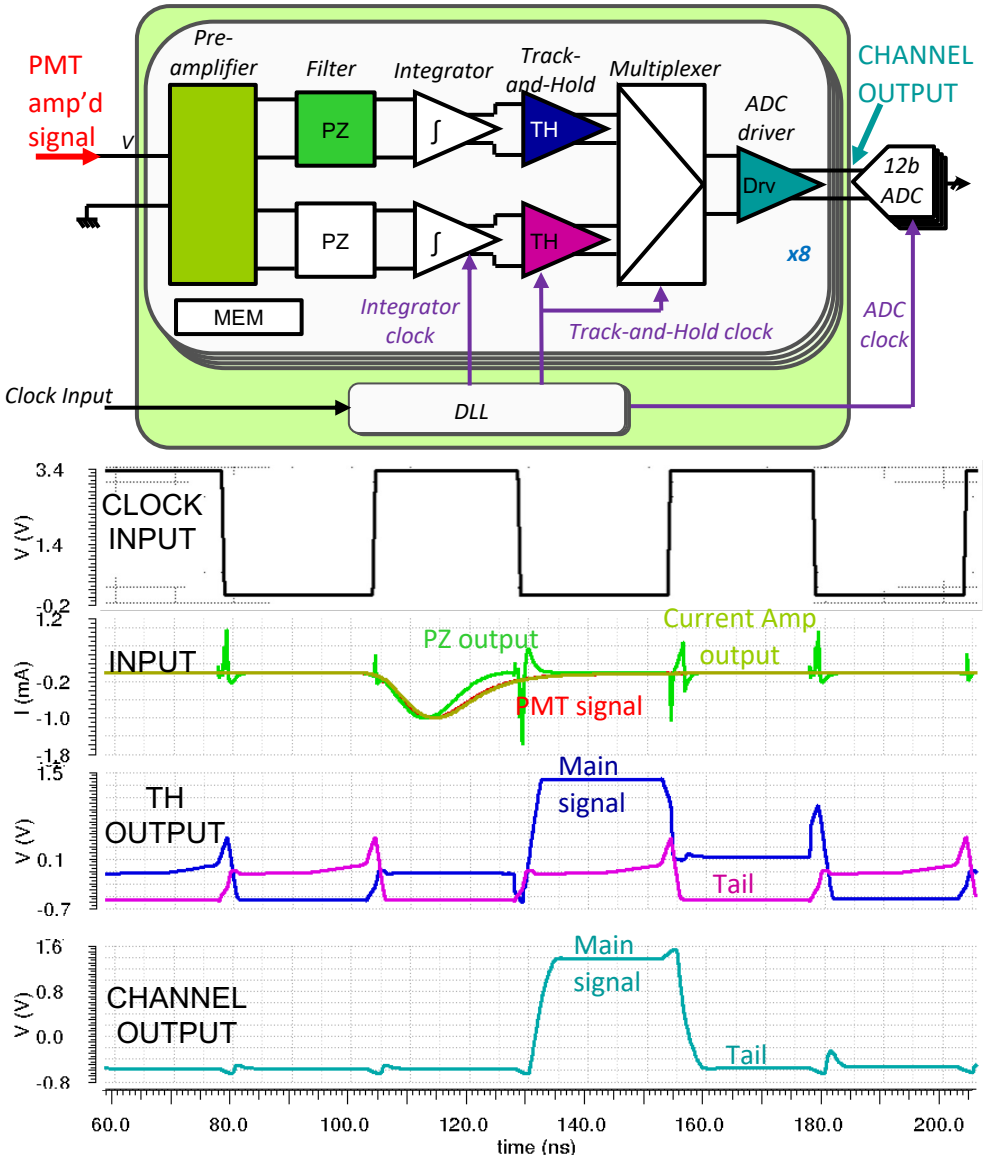






ICECAL65

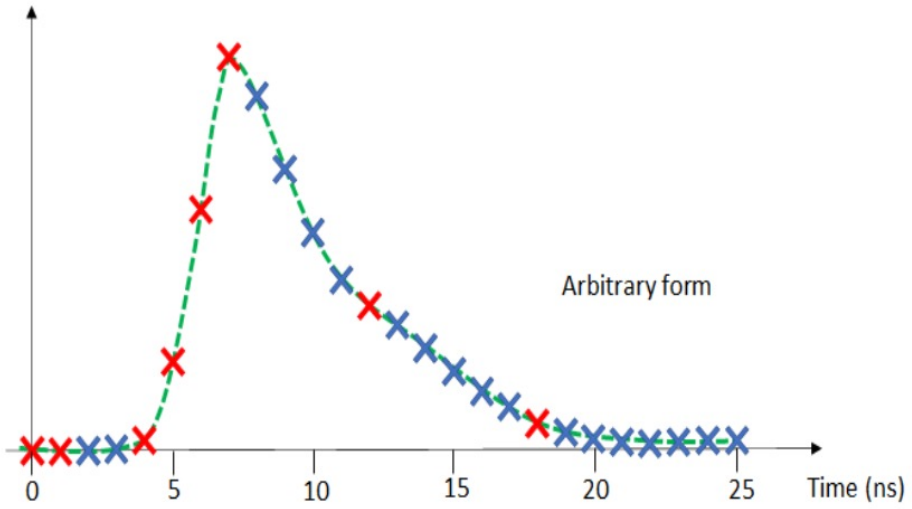
- Two separate processing paths (energy – ICECAL65 and time – SPIDER) with dedicated ASICs in CMOS 65nm TSMC technology (most lasting technology)
- Energy measurement with 2 gains to cover the large dynamic range
- Analog processing chain:
  - Input Stage:
    - low noise + high bandwidth
    - four independent signal outputs
    - extra discriminator output
  - Pole Zero cancellation Shaper:
    - minimize spillover
    - tunable pole and zero
  - Integrator:
    - tunable feedback capacitor
  - Track & Hold:
    - high slew rate
- Digital sampling synchronization
  - Dedicated DLL per channel.
  - Three independent phases for integrator, T&H and ADC.
  - Predictable subchannel after reset
- Status:
  - Channel design at behavior level ready
  - Library ready with the most essential blocks
  - OTA (for most blocks) being designed
  - DLL with 32 phase steps under design



SPIDER

Clermont/Orsay + Caen/Lyon
Tests at Syracuse of other chips

- 15ps rms resolution:
  - In range E_T = 50 MeV to 5 GeV, factor of 100
  - With maximal possible channel occupancy: the version of LS3 will aim at 10% occupancy per channel (E_T>50 MeV), improved for LS4 version
  - Based on waveform TDC (Time to Digital Convertors)
- Waveform digitization in analog memories avoids degradation of time resolution due to time walk effects when working with traditional TDC and discriminators and large dynamic ranges, but with the drawback of large readout dead-time
- Use 8 samples of the digitized wave form extract time information in a FPGA
  - Adapt easily to evolution of signal shape due to ageing
  - Compatible with timer layer option

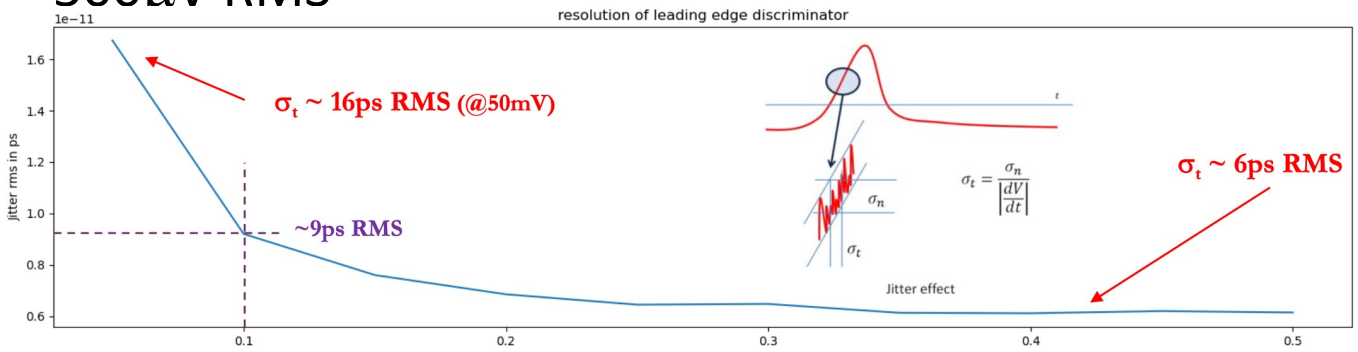


More details in Dominique Breton's talk at DRD7 ECFA workshop

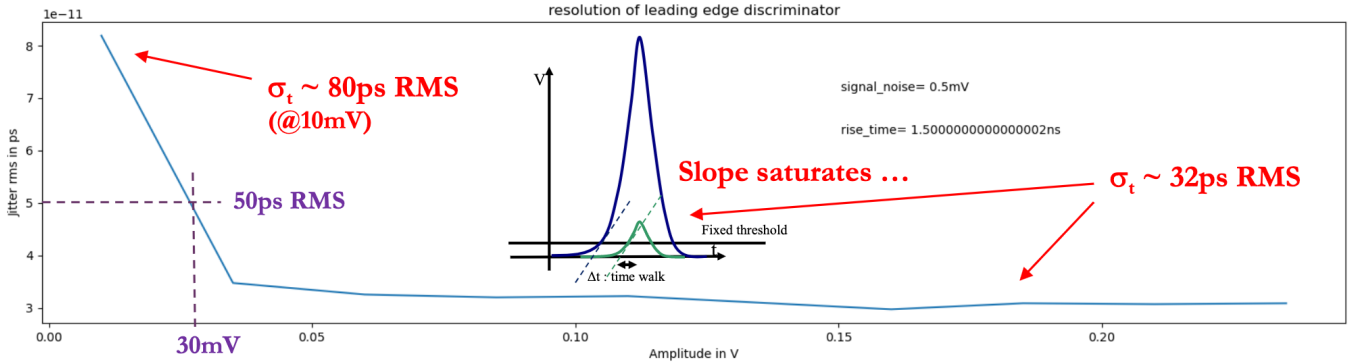
SPIDER

- Simulations of electronics timing jitter vs. signal amplitude with realistic SPACAL signal caracteristics: rise time 1.5ns, σ_{noise} = 500µV RMS

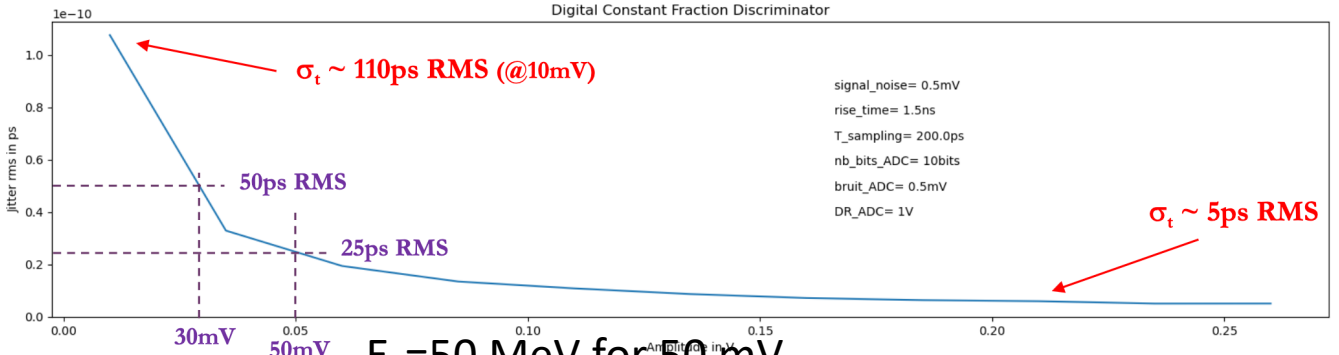
Dynamic range of 20 and TDC/single-edge discriminator



Dynamic range of 100 and TDC/single-edge discriminator



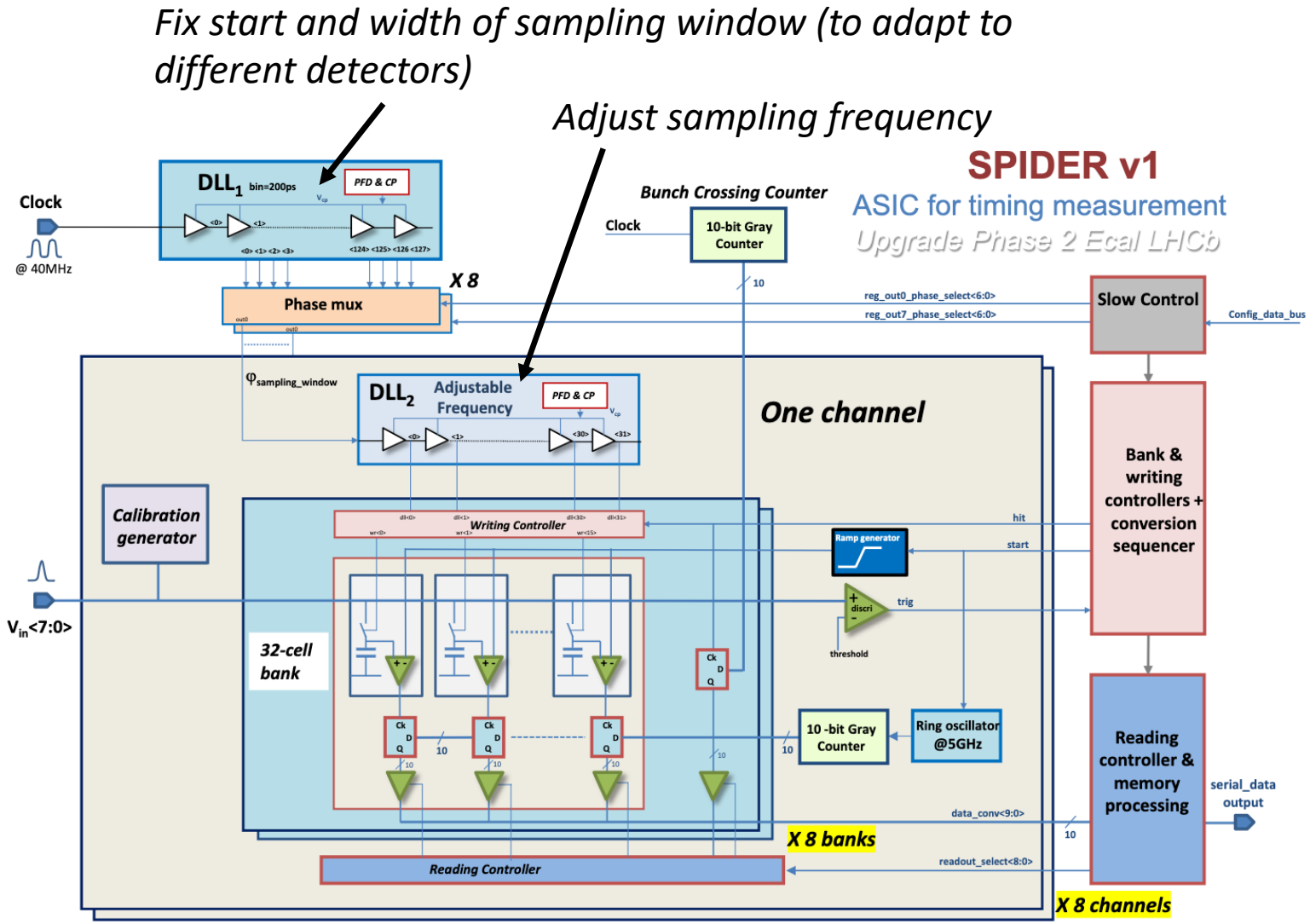
Dynamic range of 100 and SPIDER technology



E_T=50 MeV for 50 mV

SPIDER

- LS3 version:
  - 8 channels per ASIC for LS3 version
  - 8 memory banks in parallel to reduce dead-time for 10% occupancy
  - Development started in 2022
- LS4 version:
  - Add on-chip data compression
  - Get closer to 100% occupancy
  - Work with Barcelona/Valencia to try to include ICECAL in a common chip



FEBs

- Front-End board to
  - Host the two ASICs and the optical interfaces (lpGBT)
  - Perform digital processing in several FPGAs on the board (Microchip PolarFire chip)
    - time extraction,
    - pedestal subtraction,
    - Associate time and energy informations
    - Data formatting
    - Likely that more sophisticated data processing is needed in order to reduce data flow: would require communications between boards via backplane or cables
- To be largely based on previous versions produced in Orsay (9U boards, placed on the calo platform): 32 channels, 3 FEBs/PCIe40
  - Unavoidable that during Run 4 we have two different systems running in parallel
  - Because of limited space on the calo platform, need to have boards handling 64 channels for LS4, with connectors on the front and back sides
    - Need also to redesign the backplane
- Start development mid 2023

Steps for LS4

- LS3: 9344 channels in total, i.e. ~3500 extra channels (20 crates in total)
  - For 6016 channels, keep the current Run 3 electronics entire chain
  - Two options for the 3500 extra channels (x extra PCIe40/400 for both):
    - Produce 110 new FEBs (timing FEBs) with the new ASICs (ICECAL65 and SPIDER), with 32 channels per board, and interface to PCIe400:
      - Important to test precise time measurement during Run 4, even if not required for physics
    - Produce 110 FEBs (backup FEBs) almost identical to the Run 3 FEBs, using the Run 3 ICECAL ASIC but without time measurement:
      - Some components for the Run 3 FEB are not available anymore so cannot produce them identical
      - lpGBT Interface with PCIe400 (and compatible also with future PCIe40 firmwares)
- LS4: 30208 channels (24 crates in total)
  - New FEB developed for all channels, with 64 channels per board: 470 boards in total
  - With final versions of ICECAL65 and SPIDER ASICs

First planning: Chips and FEBs for LS3

- PMT conditioning chip: produced and tested end of 2025
- ICECAL65: v0 (8 channels) mid 2025, v1 (16 channels) end of 2027
- SPIDER: v0 (2 channels) mid 2024, v1 (8 channels) mid 2026, v2 (LS3) end of 2027
- FEBs:
  - R&D of the timing and backup FEBs in parallel until 2026
  - Decide beginning of 2026 which one to produce for Run 4:
    - To produce *timing FEB*, we need to wait for the production of the ASICs: FEBs would be produced and tested end of 2028
    - For the *backup FEBs*, they would be ready mid 2027. Possibility to install still a smaller number of timing FEBs during on YETS of Run 4 to test the timing

PCIe400

- For LS3, keep data processing similar to Run 3, i.e. send all energy measurement offline + 10% of the time measurement (removing LLT):
  - Requires extra 20 PCIe40 or 10 PCIe400
  - 440 extra optical links
- For LS4, some data processing to reduce the data flow will be necessary, which can be done partly in the PCIe400 FPGAs
  - Some ideas for FPGA assisted co-processing presented by Riley Henderson (Monash University) in December
- LAPP Annecy agrees to take care of the basic data processing firmware (similar to the Run 3 one), help needed for the development of the more complex options for LS4

Open tasks

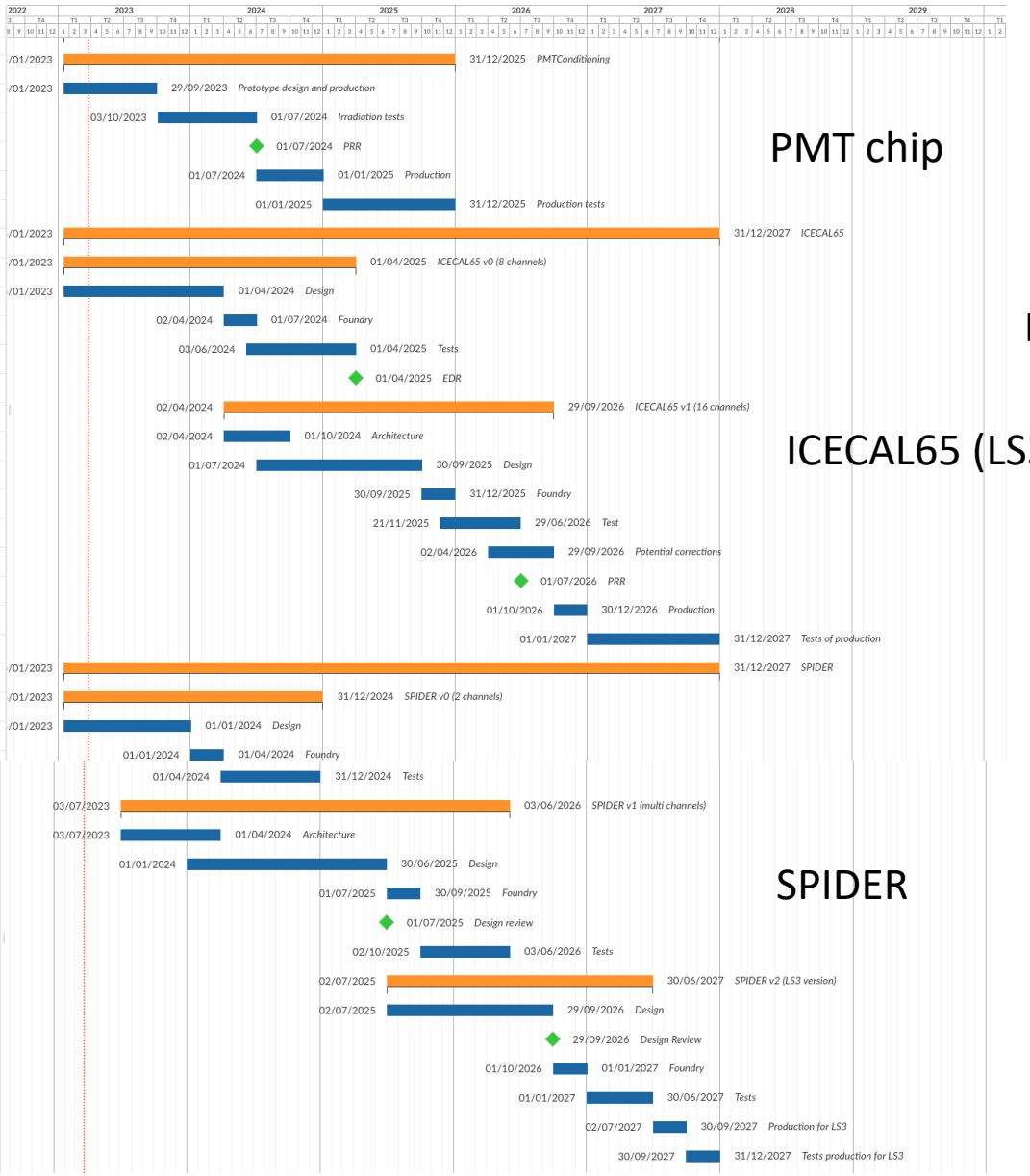
- Second test bench for SPIDER (Syracuse potentially interested)
- Backplanes of Front-End crates and the associated connectics for LS4
- Analog cables (signal, interconnections)
- Optical connections
- Power-supplies for Front-End crates
- Electronics for calibration system (LEDs, Cincinnati potentially interested)
- Software for slow control of the electronics
- Firmware for advanced data processing in PCIe400 (or FEB)

Conclusions

- Architecture defined for the electronics chain, for energy and time measurement
- R&D for 2 ASICs to measure energy and time started last year, R&D for FEB starting now
- Planning to have these 2 ASICs already in Run 4 (which would allow to test timing with the Calo) is tight, but the associated developments are required also for LS4
- Realistic back-up plan also in place with contingency to be ready and commissioned for the start of Run 4

Chip planning

SUJET	DATE DE DÉBUT	DATE DE FIN	ID
ASICS	16/01/2023	31/12/2027	43
PMTConditioning	16/01/2023	31/12/2025	102
Prototype design and ...	16/01/2023	29/09/2023	103
Irradiation tests	03/10/2023	01/07/2024	104
PRR	01/07/2024	01/07/2024	106
Production	01/07/2024	01/01/2025	107
Production tests	01/01/2025	31/12/2025	108
ICECAL65	16/01/2023	31/12/2027	45
ICECAL65 v0 (8 chann...	16/01/2023	01/04/2025	90
Design	16/01/2023	01/04/2024	92
Foundry	02/04/2024	01/07/2024	93
Tests	03/06/2024	01/04/2025	94
EDR	01/04/2025	01/04/2025	95
ICECAL65 v1 (16 chan...	02/04/2024	29/09/2026	91
Architecture	02/04/2024	01/10/2024	96
Design	01/07/2024	30/09/2025	97
Foundry	30/09/2025	31/12/2025	98
Test	21/11/2025	29/06/2026	99
Potential correctio...	02/04/2026	29/09/2026	101
PRR	01/07/2026	01/07/2026	100
Production	01/10/2026	30/12/2026	50
Tests of production	01/01/2027	31/12/2027	51
SPIDER	16/01/2023	31/12/2027	52
SPIDER v0 (2 channels)	16/01/2023	31/12/2024	74
Design	16/01/2023	01/01/2024	53
Foundry	01/01/2024	01/04/2024	76
Tests	01/04/2024	31/12/2024	77
SPIDER v1 (multi chan...	03/07/2023	03/06/2026	78
Architecture	03/07/2023	01/04/2024	80
Design	01/01/2024	30/06/2025	81
Foundry	01/07/2025	30/09/2025	83
Design review	01/07/2025	01/07/2025	82
Tests	02/10/2025	03/06/2026	84
SPIDER v2 (LS3 versio...	02/07/2025	30/06/2027	79
Design	02/07/2025	29/09/2026	85
Design Review	29/09/2026	29/09/2026	86
Foundry	01/10/2026	01/01/2027	87
Tests	01/01/2027	30/06/2027	88
Production for LS3	02/07/2027	30/09/2027	89
Tests production for L...	30/09/2027	31/12/2027	105



PMT chip

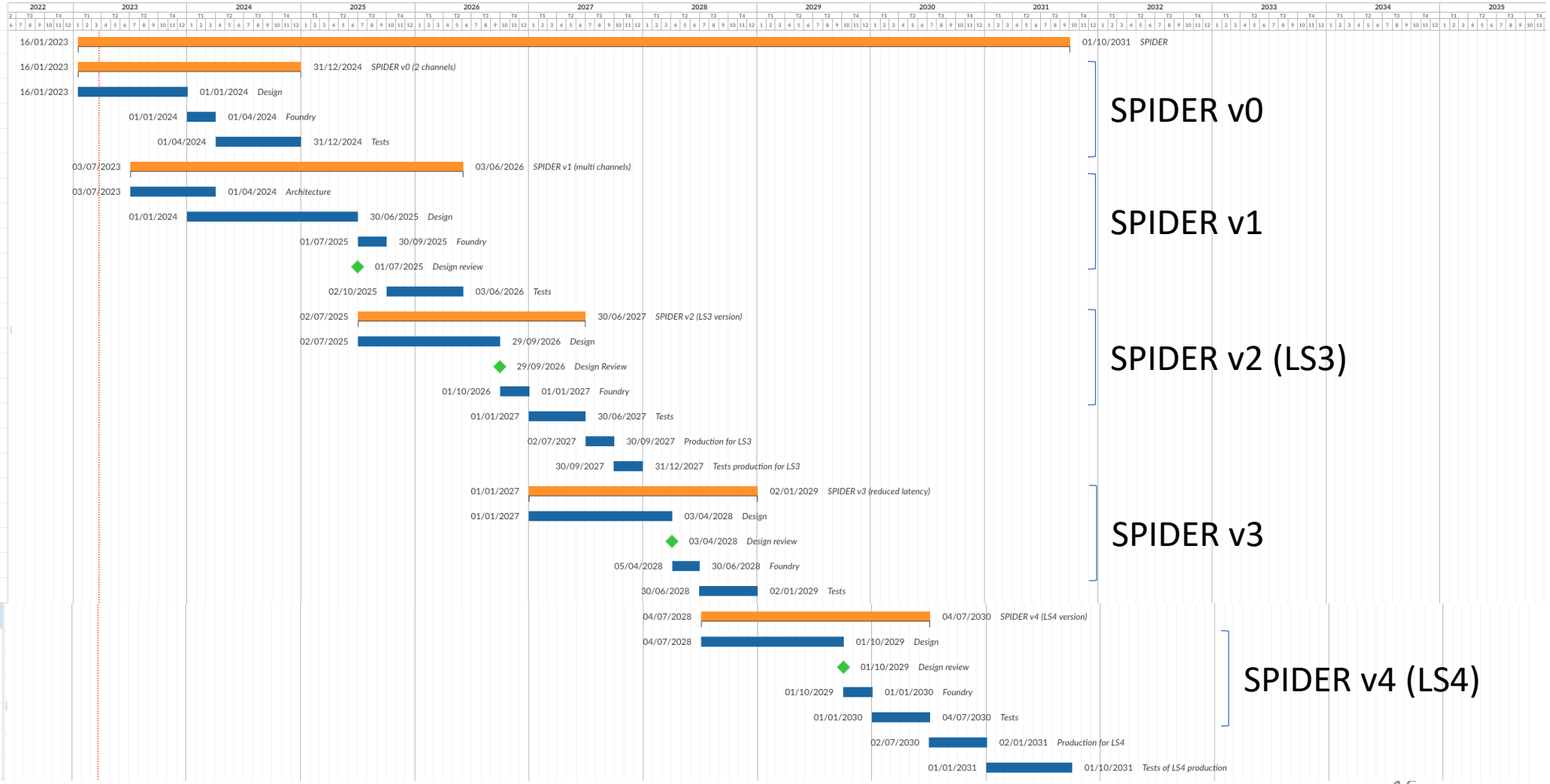
ICECAL65 (LS3 version is final one)

SPIDER

End of production + tests = End of 2027

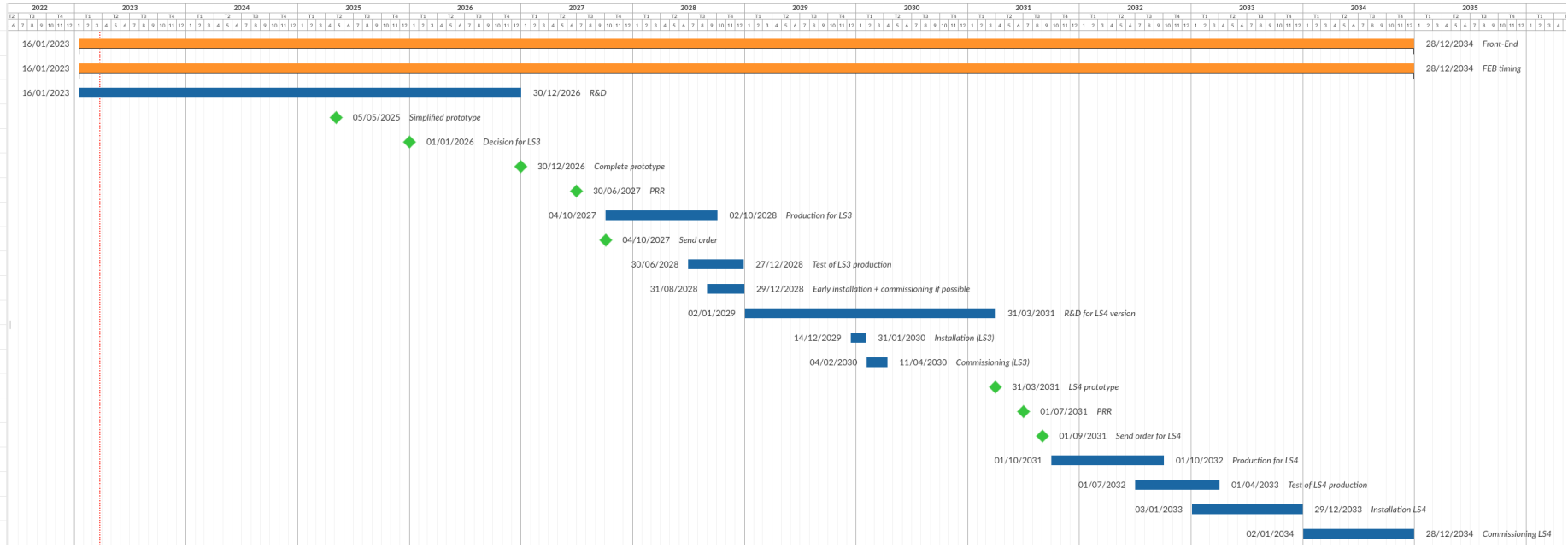
SPIDER: Planning for LS4

SUJET	DATE DE DÉBUT	DATE DE FIN
SPIDER	16/01/2023	01/10/2031
SPIDER v0 (2 channels)	16/01/2023	31/12/2024
Design	16/01/2023	01/01/2024
Foundry	01/01/2024	01/04/2024
Tests	01/04/2024	31/12/2024
SPIDER v1 (multi channels)	03/07/2023	03/06/2026
Architecture	03/07/2023	01/04/2024
Design	01/01/2024	30/06/2025
Foundry	01/07/2025	30/09/2025
Design review	01/07/2025	01/07/2025
Tests	02/10/2025	03/06/2026
SPIDER v2 (LS3 version)	02/07/2025	30/06/2027
Design	02/07/2025	29/09/2026
Design Review	29/09/2026	29/09/2026
Foundry	01/10/2026	01/01/2027
Tests	01/01/2027	30/06/2027
Production for LS3	02/07/2027	30/09/2027
Tests production for LS3	30/09/2027	31/12/2027
SPIDER v3 (reduced latency)	01/01/2027	02/01/2029
Design	01/01/2027	03/04/2028
Design review	03/04/2028	03/04/2028
Foundry	05/04/2028	30/06/2028
Tests	30/06/2028	02/01/2029
SPIDER v4 (LS4 version)	04/07/2028	04/07/2030
Design	04/07/2028	01/10/2029
Design review	01/10/2029	01/10/2029
Foundry	01/10/2029	01/01/2030
Tests	01/01/2030	04/07/2030
Production for LS4	02/07/2030	02/01/2031
Tests of LS4 production	01/01/2031	01/10/2031



FEB planning: timing FEB (LS4) and backup FEB (LS3)

SUJET	DATE DE DÉBUT	DATE DE FIN
Front-End	16/01/2023	28/12/2034
FEB timing	16/01/2023	28/12/2034
R&D	16/01/2023	30/12/2026
Simplified prototype	05/05/2025	05/05/2025
Decision for LS3	01/01/2026	01/01/2026
Complete prototype	30/12/2026	30/12/2026
PRR	30/06/2027	30/06/2027
Production for LS3	04/10/2027	02/10/2028
Send order	04/10/2027	04/10/2027
Test of LS3 production	30/06/2028	27/12/2028
Early installation + commissioning ...	31/08/2028	29/12/2028
R&D for LS4 version	02/01/2029	31/03/2031
Installation (LS3)	14/12/2029	31/01/2030
Commissioning (LS3)	04/02/2030	11/04/2030
LS4 prototype	31/03/2031	31/03/2031
PRR	01/07/2031	01/07/2031
Send order for LS4	01/09/2031	01/09/2031
Production for LS4	01/10/2031	01/10/2032
Test of LS4 production	01/07/2032	01/04/2033
Installation LS4	03/01/2033	29/12/2033
Commissioning LS4	02/01/2034	28/12/2034



SUJET	DATE DE DÉBUT	DATE DE FIN
FEB backup	16/01/2023	01/01/2029
R&D	16/01/2023	09/04/2025
Simplified prototype	31/01/2024	31/01/2024
Complete prototype	09/04/2025	09/04/2025
EDR (both FEBs)	06/05/2025	06/05/2025
Decision for LS3	01/01/2026	01/01/2026
PRR	01/01/2026	01/01/2026
Send order	01/01/2026	01/01/2026
Production	01/01/2026	29/12/2026
Tests of production	01/01/2027	01/07/2027
Installation	01/07/2027	03/01/2028
Commissioning	03/01/2028	01/01/2029