Mighty Tracker CMOS

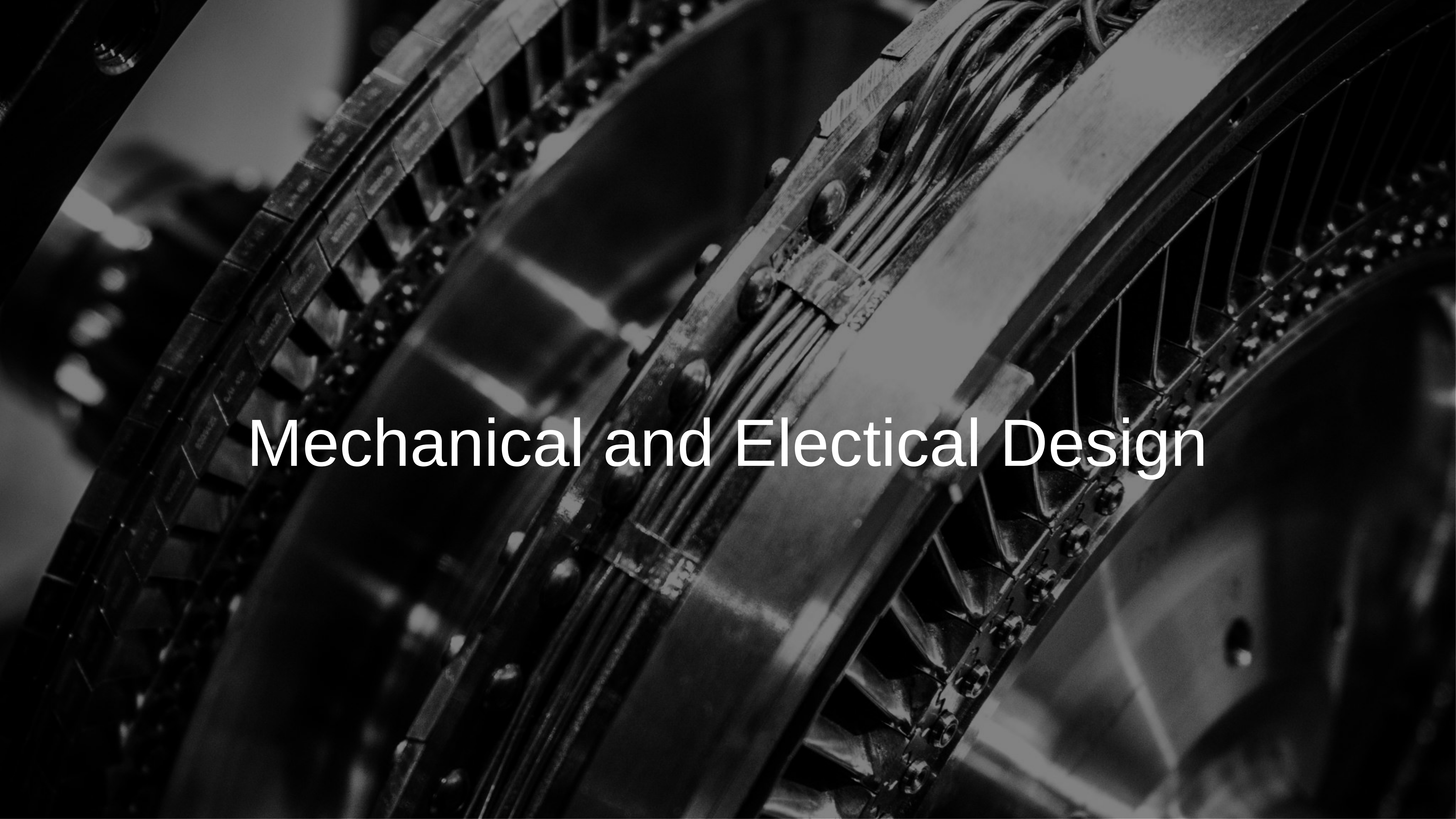
Klaas Padeken

HV-CMOS

- One of the main drivers of the project is the size of the silicon area
- MAPS chips are limited to ~2x2 cm^2 (foundry)
- The most critical points are:
  - In Time **Efficiency**
  - **Power** Consumption
  - **Radiation** Tolerance

Pixel size	< 100 µm x 300 µm
In-time efficiency	> 99% within 25 ns window
Timing resolution	~ 3 ns within 25 ns window
Radiation tolerance	6×10^{14} 1 MeV n_{eq}/cm^2
Power consumption	< 150 mW/cm^2
Data transmission	4 links of 1.28 Gb/s each
Compatibility with the LHCb readout system	

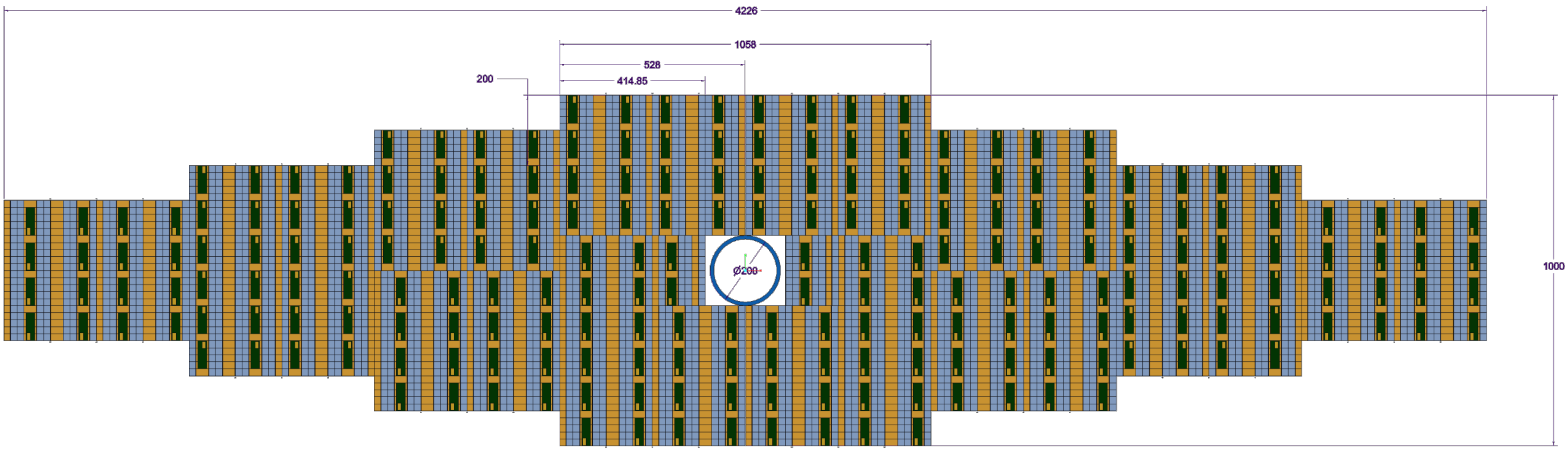
LHCb-INT-2019-007, 2019



Mechanical and Electical Design

Mechanical Layout

One Layer 3m^2
2 Layers per station
6 Layers in total

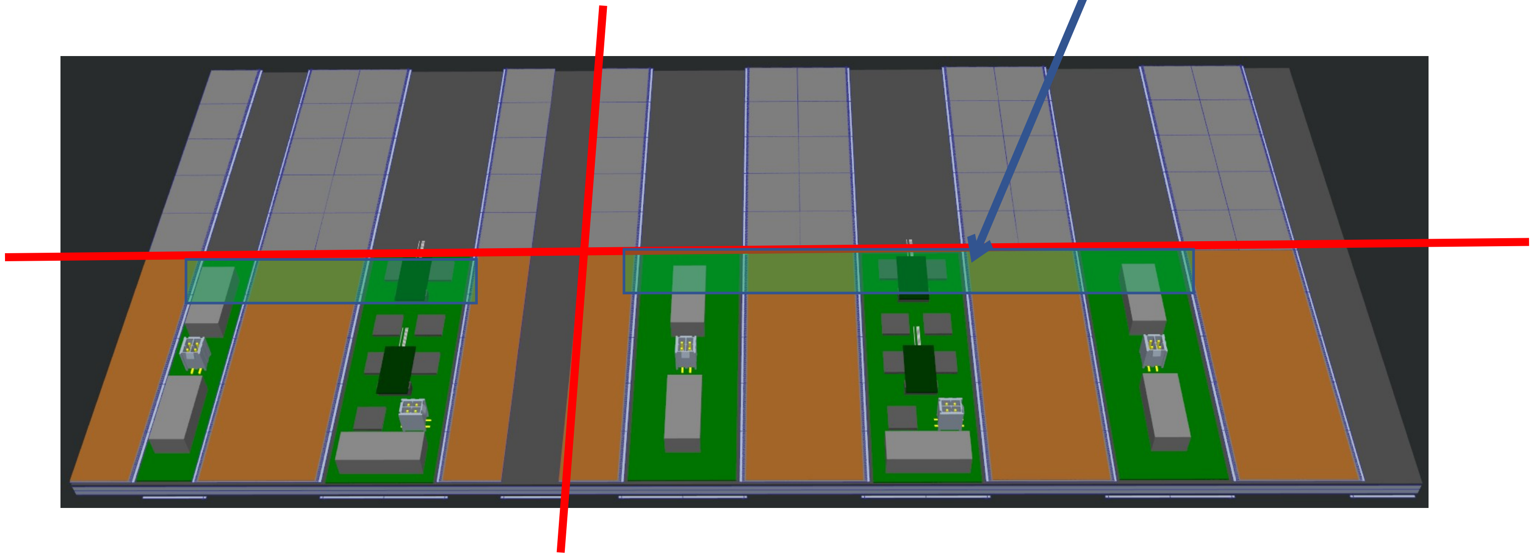


- Module height given by the beamhole (20cm)
- Shape follows the highest acceptable occupancy in the fiber region
- Width is fixed to ~53cm for multiples of 2cm (chip) + overlap

Modules

Sub-module type	MightyPix	lpGBT	VTRx+
B	35	3	1
C	35	5	2
D	20	7	2

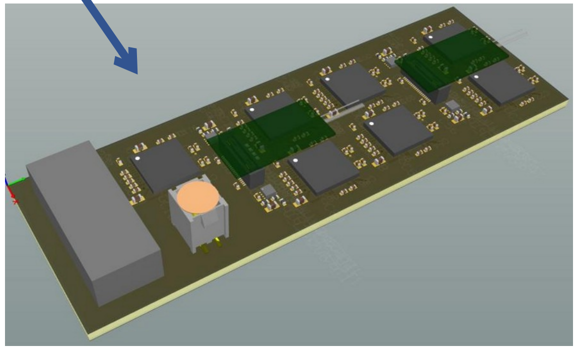
co-cured flex

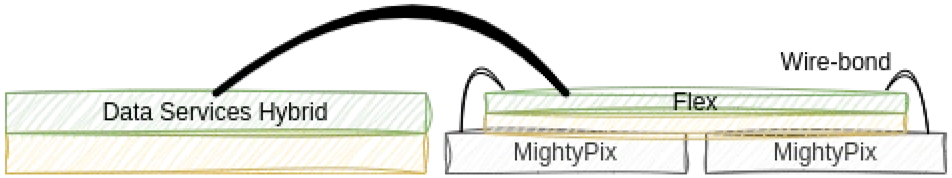


Short sub-module

Long sub-module

- One layer consists of 4 sub-modules
- 28 modules per layer (2 short)
- One sub-module is a electrical unit
- Build chip-modules to save space
- Co-cured service flex for power/signal distribution





Ongoing space/power optimization

DAQ concept

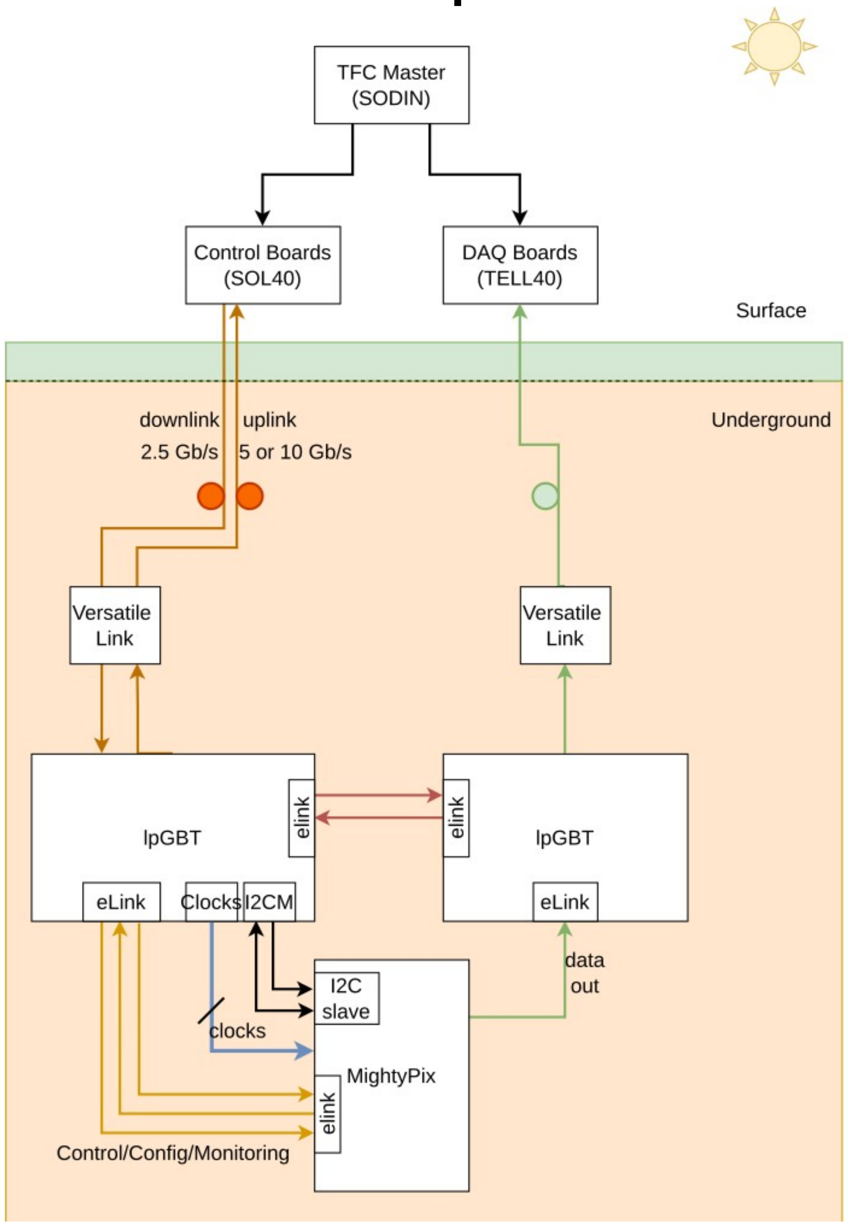


Diagram from Karol Hennessy

"Classical" DAQ design

Separation of Control (SOL40) and Data output (Tell40)

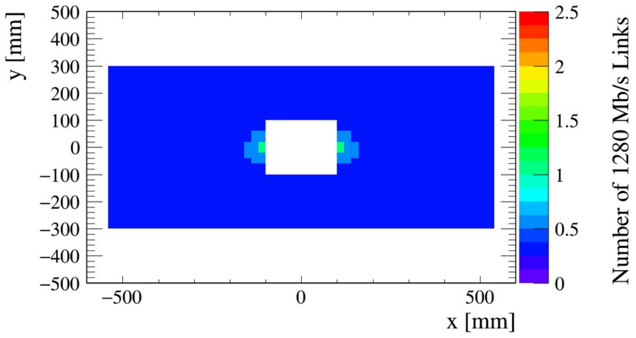
This will be one of the big challenges for U2

One interesting feature:

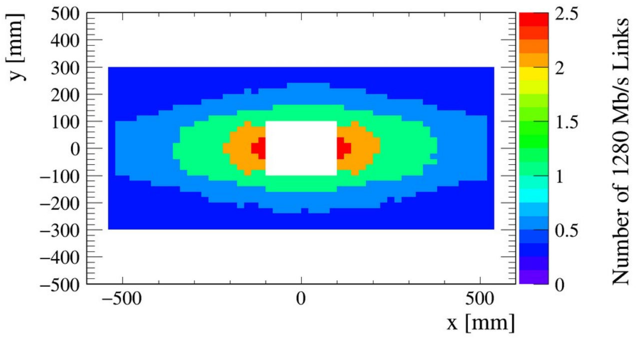
The readout **speed and number of links** will be be **adjusted** to the expected occupancy

Hottest chip: 1.7hits/25ns → 17MHz/cm^2 ~3Gb/s

LS3



Upgrade 2



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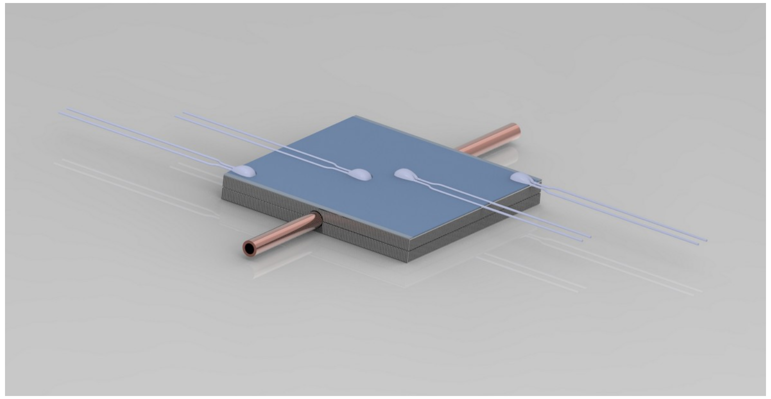
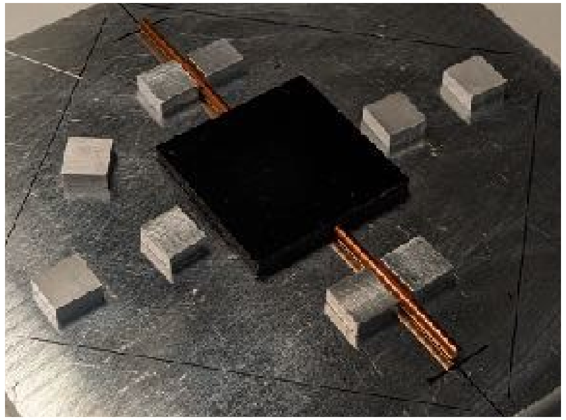
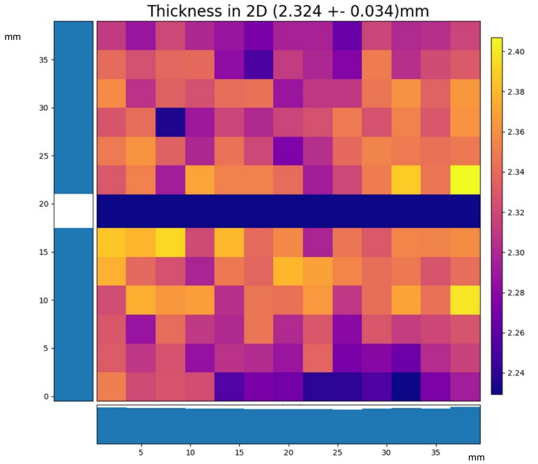
https://indico.cern.ch/event/1249629/

Module Prototyping

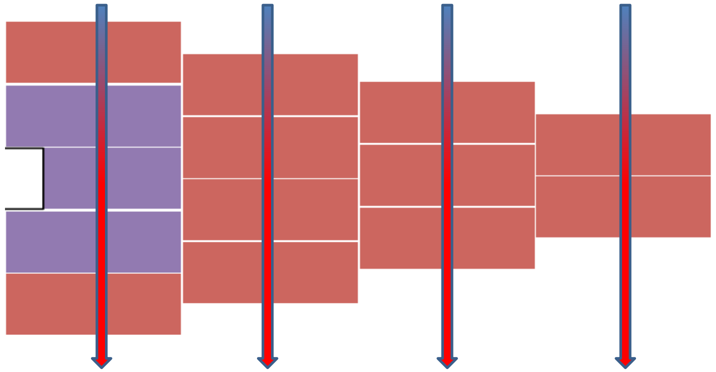


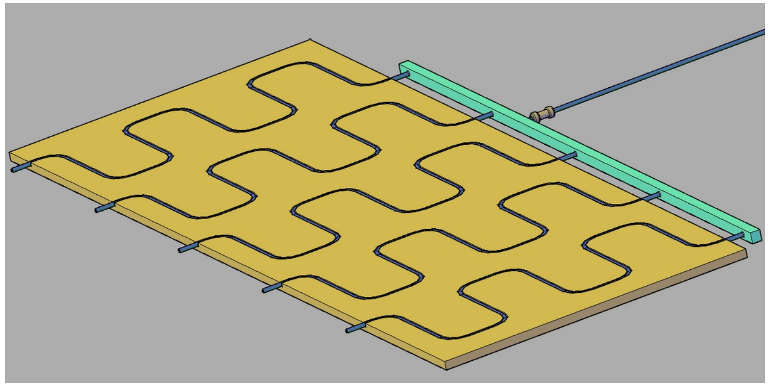




- First co-cured module done
- Good first thickness variation (expected to get better)
- Problem procuring CF-foam (same for all LHC experiments)
- Thermal tests ongoing

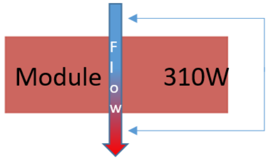
Critical Item: Cooling





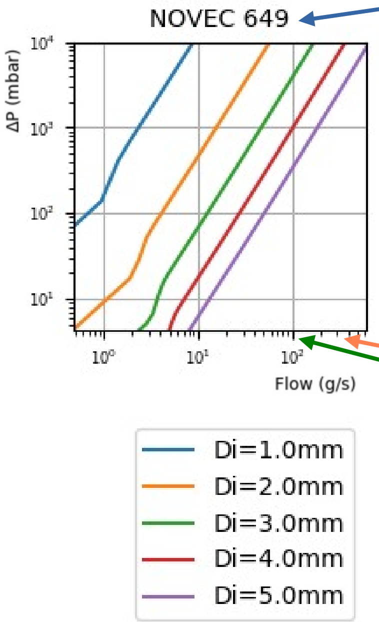
Worse Case Scenario:
150mW/cm² (safety,DCDC) → 300mW/cm²
1 Layer 3m² → 9kW
3 Stations with 2 layers → 54kW

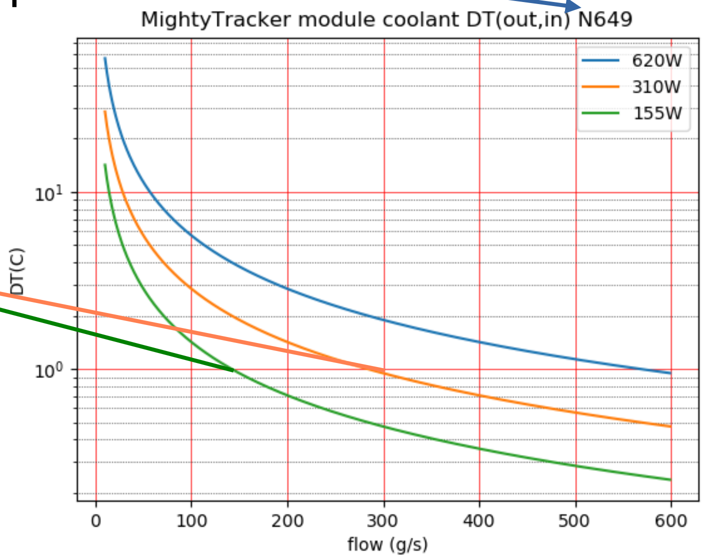
Very optimistic Scenario:
100mW/cm² → 150mW/cm²
1 Layer 3m² → 4.5kW
3 Stations with 2 layers → 27kW



- There is a big amount of heat, that needs to be cooled
- Several approaches are studied
- Big impact from the operation temperature and the chip power consumption
- Try to stay with monophase cooling (if possible)

We know the problem





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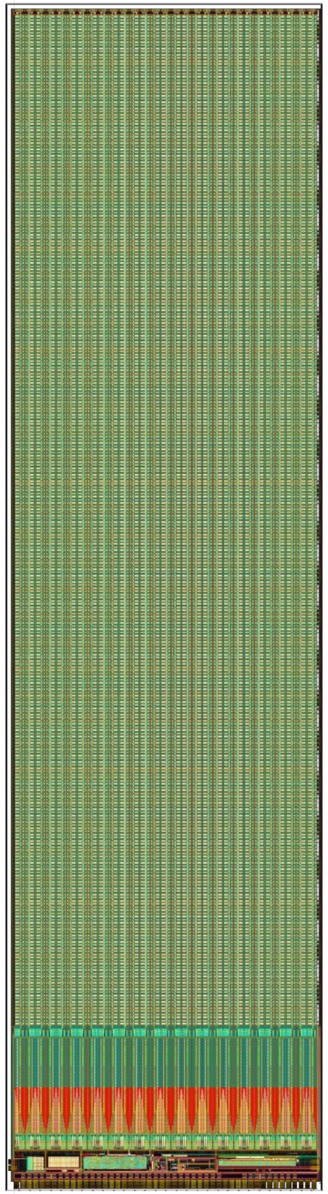
https://indico.cern.ch/event/971149/
https://indico.cern.ch/event/922623/
https://indico.cern.ch/event/1006101/

HVCMOS Sensor Design

MightyPix1 Design

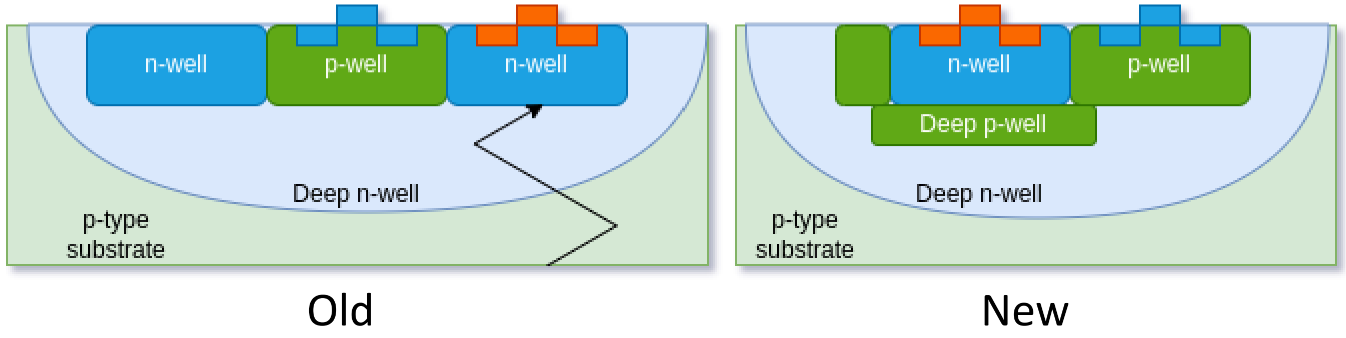
- Chip size: 5 x 20 mm^2
- Pixel matrix: 29 x 320
- Pixel:
  - 55 x 165 μm^2
  - CMOS amplifier and CMOS comparator (~3ns Resolution)
  - Data format: 2 x 32bit per Hit
  - Digital Interfaces:Timing and Fast Control (TFC)
  - Slow Control (I2C)
  - Shift-Register Interface (SR)
  - Clock Generation:
  - External: 640 MHz and 40 MHz from lpGBT
  - Internal: CML and CMOS PLL with 40 MHz reference clock (planned to be used in LHCb)
- Bias Voltages:
  - Integrated 10bit voltage DACs
  - Supplied externally
  - HV > 120V possible
- Data output 1 x 1.28Gbit/640Mbit/320Mbit
- NIEL 3-6 x 10^{14} n_{eq}/cm^2

Layout for MightyPix1 (1/4 of full size)

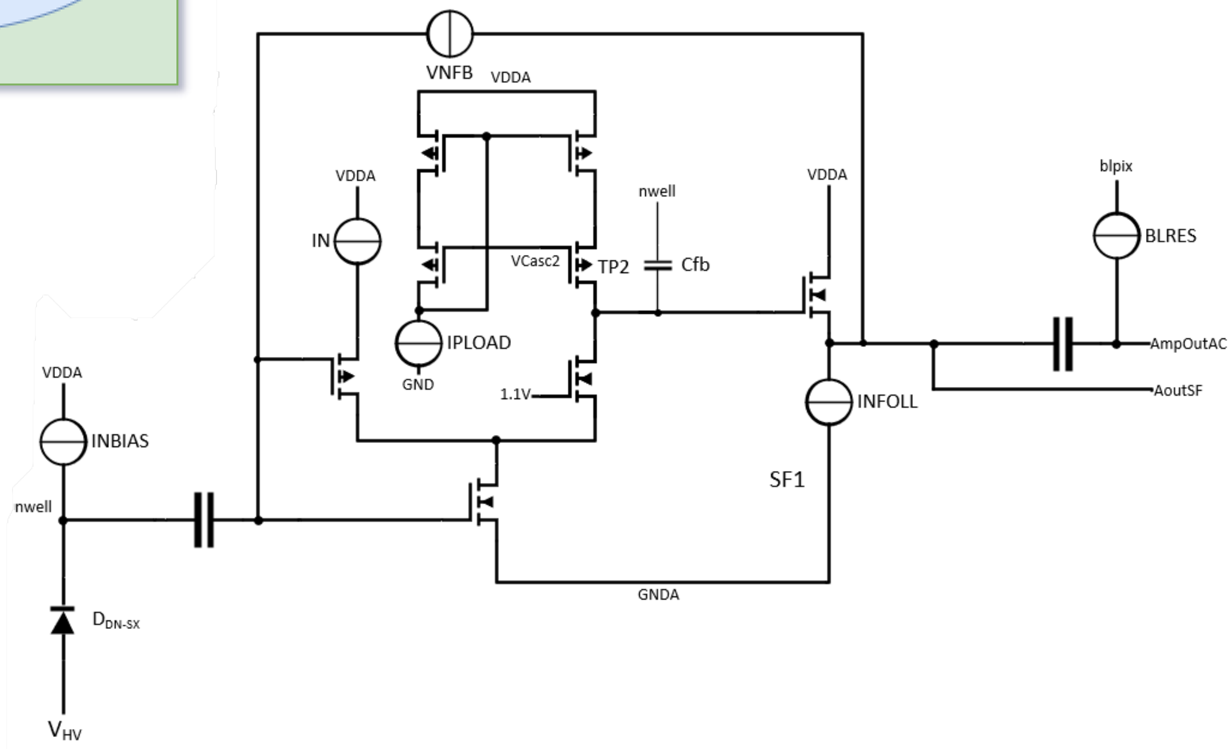


CMOS Amplifier/Comparator

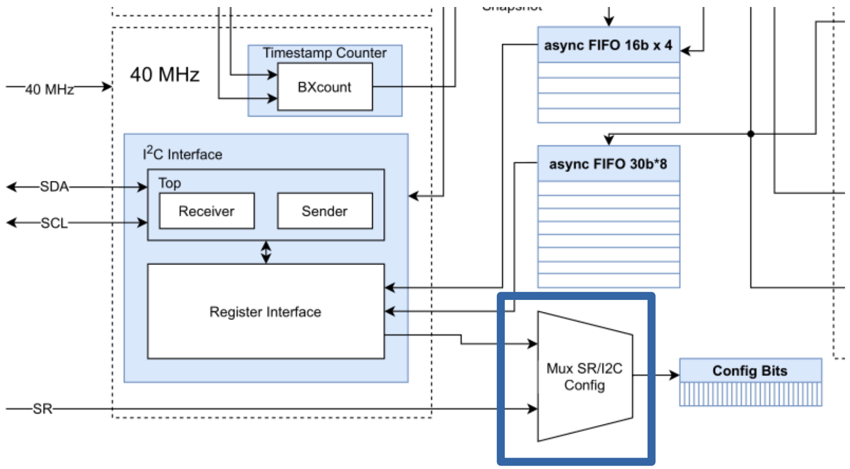
New deep p-well enables the use of CMOS amplifier and comparator in the pixel cell



- CMOS style amplifier
- ENC: 67 e^- (88 fF pixel capacitance)
- Timewalk: 2.4 ns for signals from
- 2400 e^- to 24000 e^-



Problems with MightyPix1



- There was a mistake in the MP1 design
- New I2C interface and the well tested shift register interfered
- One load signal not connected (Bias block)
- Sadly the simulation tested after config block
- An error message was overlooked

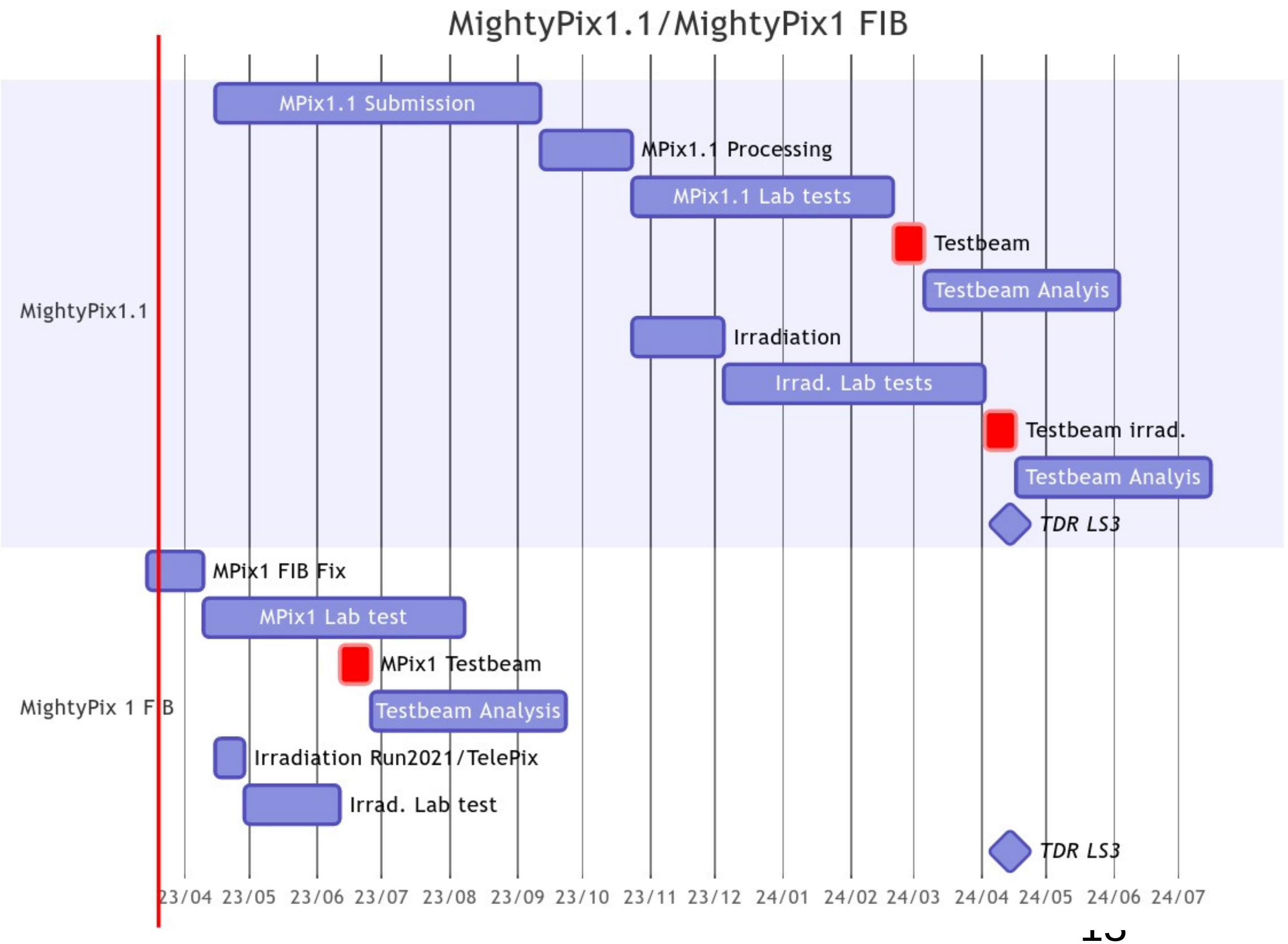
- Things happen. We will now concentrate on what to do!

Table B.2: 36 IDACs

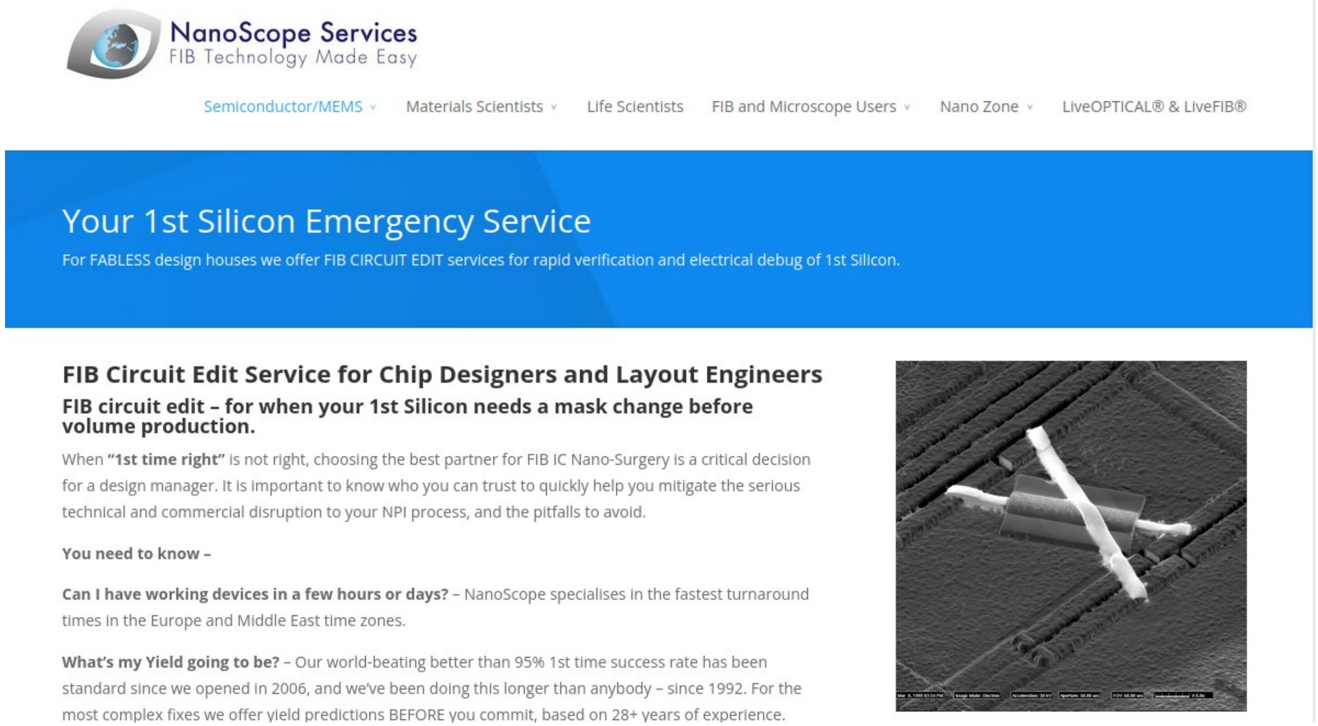
DAC	Bits	Default
Q0	1:0	0
Qon	3:0	4'b0101
BLRes	5:0	6'd5
VNCompFine	5:0	6'd1
VN	5:0	6'd20
VNFB	5:0	6'd5
VNRegC	5:0	6'd1
VNDel	5:0	6'd10
VPBigFine	5:0	6'd20
VPDAC	5:0	0
VN	5:0	0
VNFoll2	5:0	6'd20
VNFB2	5:0	0
VPLoad2	5:0	0
VPVCO	5:0	6'd7
VNVCO	5:0	6'd15
VPDelDclMux	5:0	6'd30
VNDelDclMux	5:0	6'd30
VPDelDcl	5:0	6'd30
VNDelDcl	5:0	6'd30
VPDelPreEmp	5:0	6'd30
VNDelPreEmp	5:0	6'd30
VPDcl	5:0	6'd30
VNDcl	5:0	6'd30
VNLVDS	5:0	6'd10
VNLVDSDel	5:0	6'd10
VPPump	5:0	6'd5
VNCPc	5:0	6'd5
VNVCOc	5:0	6'd10
VPRegCasc	5:0	0
VPSmallFine	5:0	6'd20
VNComp	5:0	6'd30
VPFoll	5:0	6'd30
VPBiasRec	5:0	6'd5
VNBiasRec	5:0	6'd5

Resubmission

- KIT offered to resubmit a fixed MightyPix1.1
- Consider using repaired sensors (Focused Ion Beam FIB)
- Maybe wafer scale or more FIB is possible



Focused Ion Beam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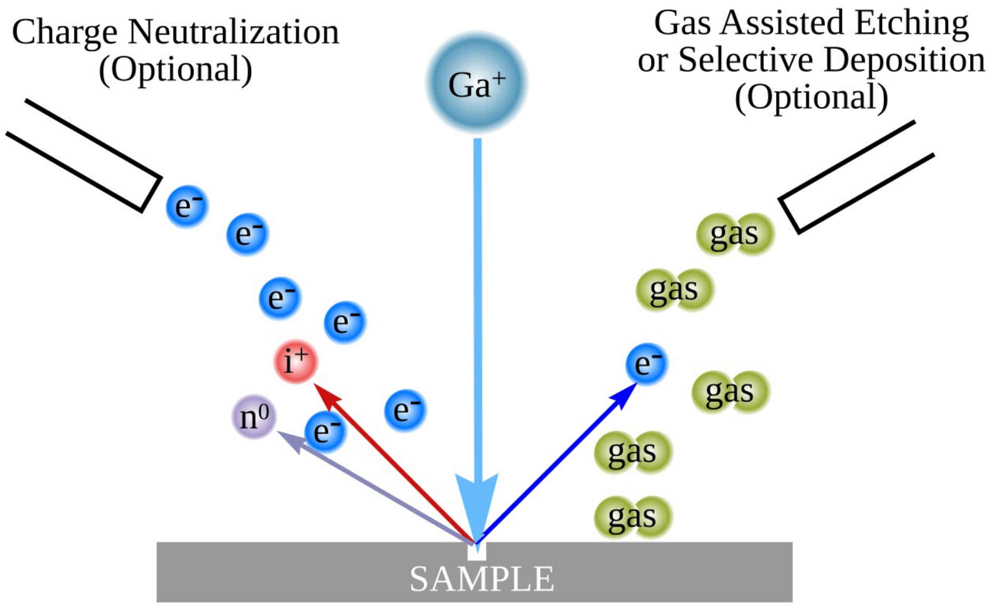
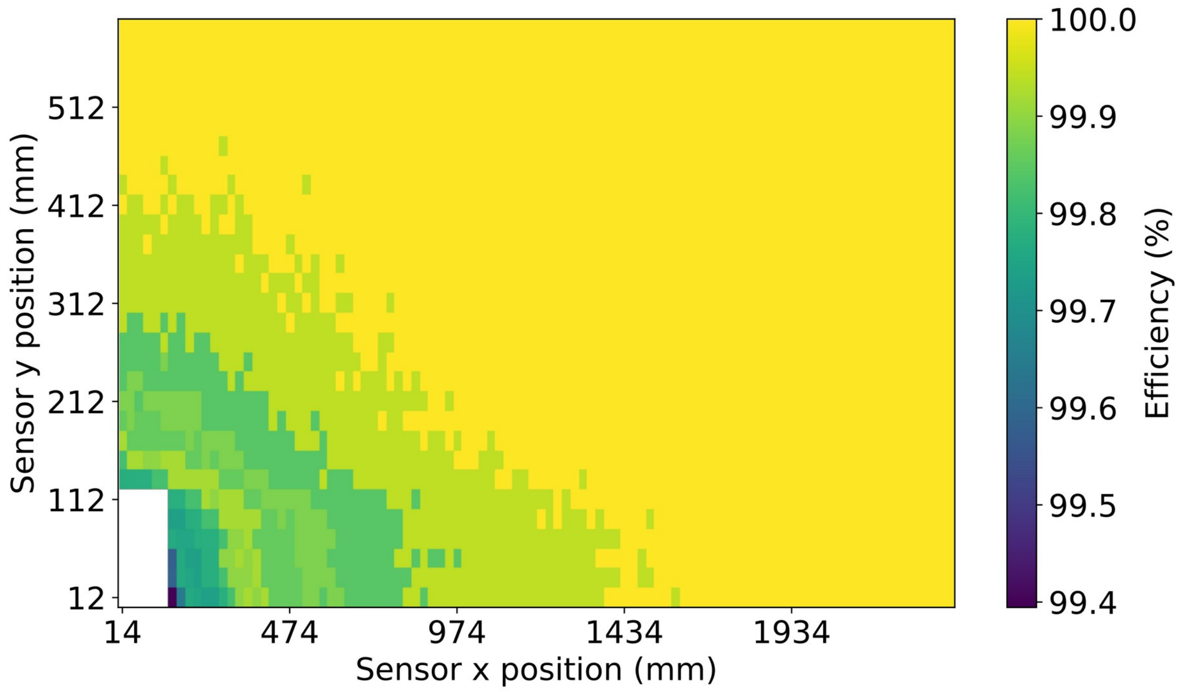


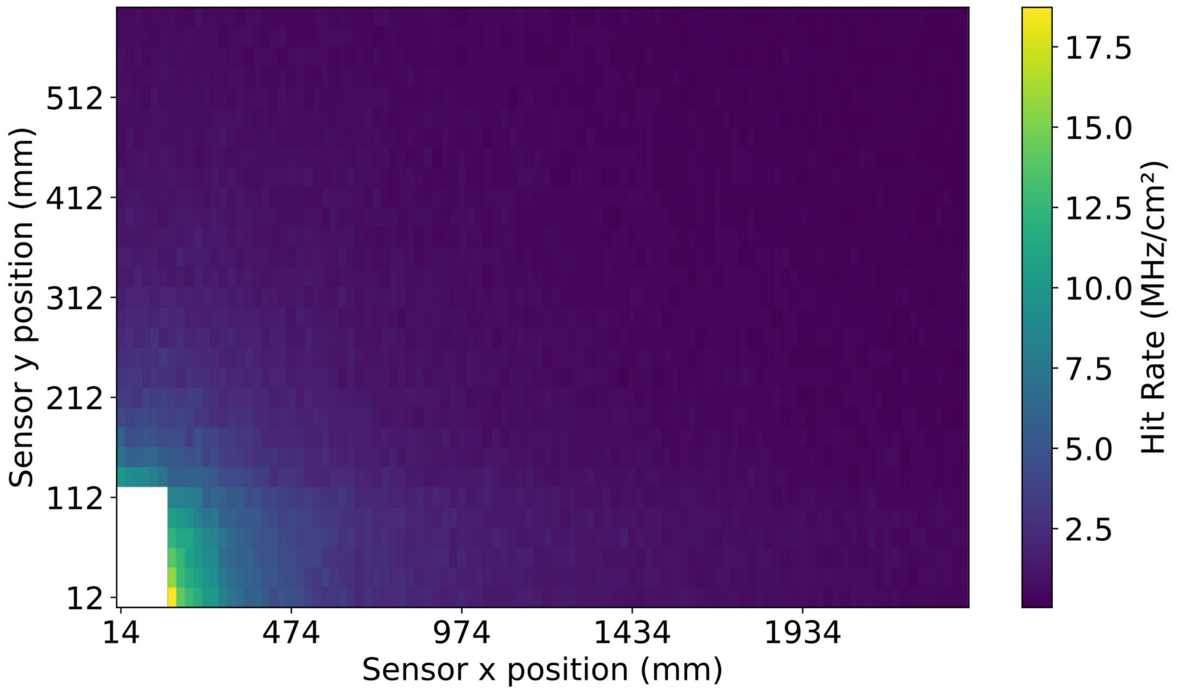
[Souce Wikipedia]

First samples are "repaired" (cutting and adding new line)
Plan to repair more samples (more experimental less expensive)

Current Status of the Sensor

Hit rate



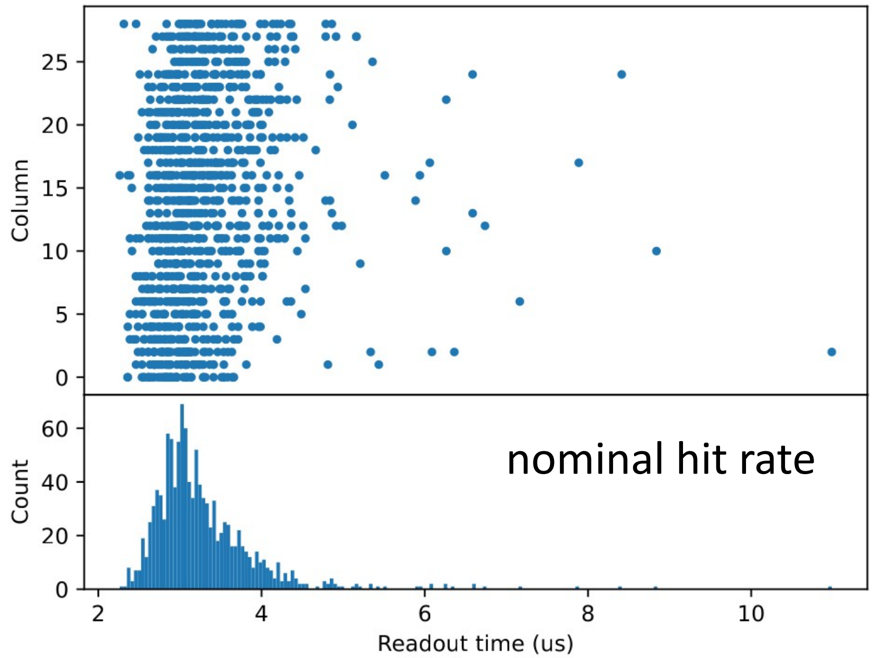


Max hit rate 17MHz/cm^2

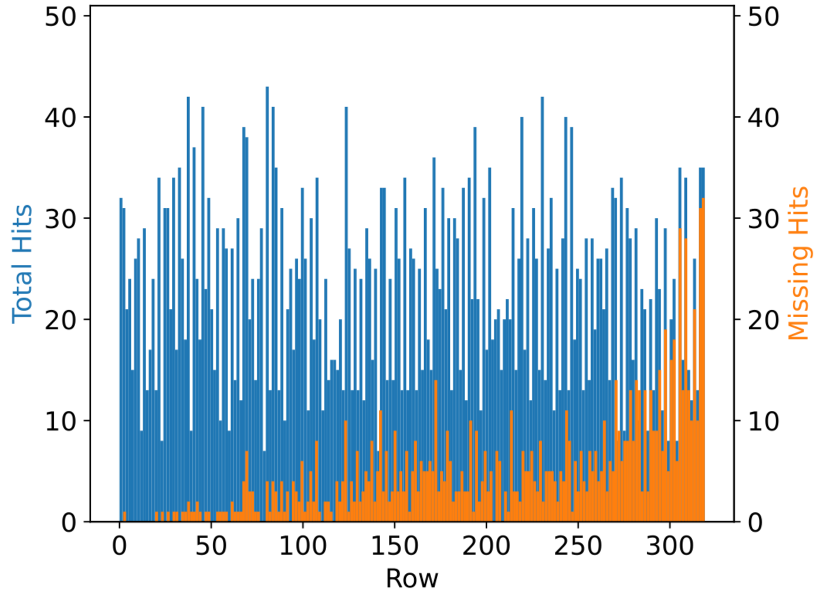
The simulation of the MightyPix FSM readout efficiency.
Limited at the moment by statistics.
→ But even in simulation not 100% efficient, but close to it.

https://indico.cern.ch/event/1269648/

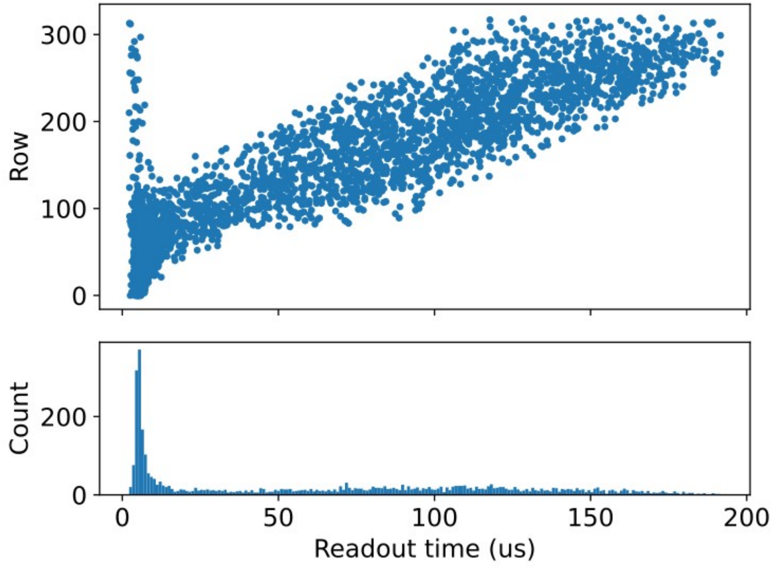
Maximum hit rate



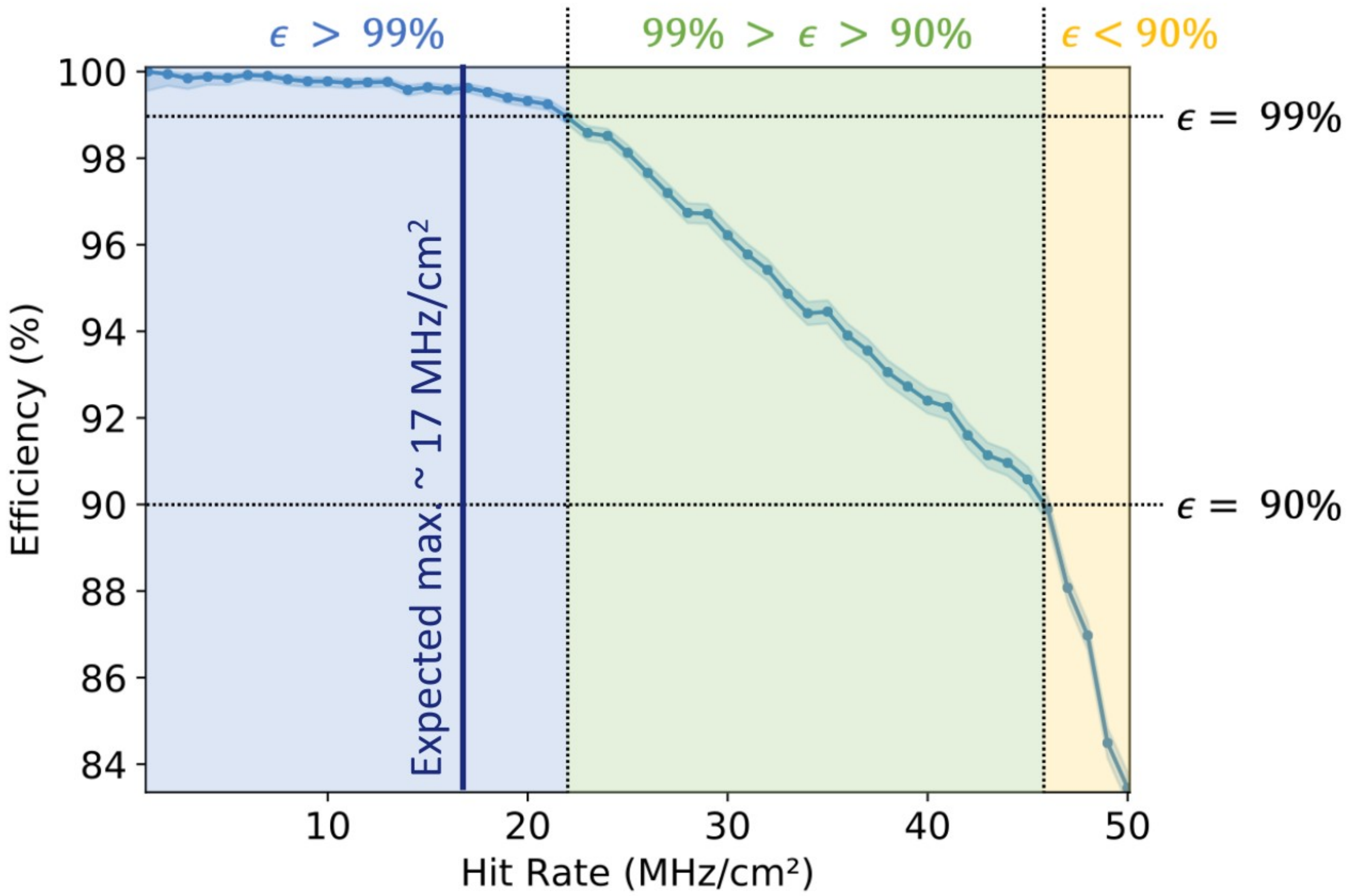
Simulation provides a realistic readout time
Main source of missing hits are two hits in the same pixel
Before the hits can not be associated to the correct BX, they are trapped in the readout and never leave the sensor.
Readout delay is dominated by the column readout (worse case fixed TOT of 2µs used here)



4x nominal hit rate (68 MHz)



Are we at some edge?



- This would be good enough for the current simulated Hit rate, but no margin left
- The single hitbuffer per column was identified as the main bottleneck

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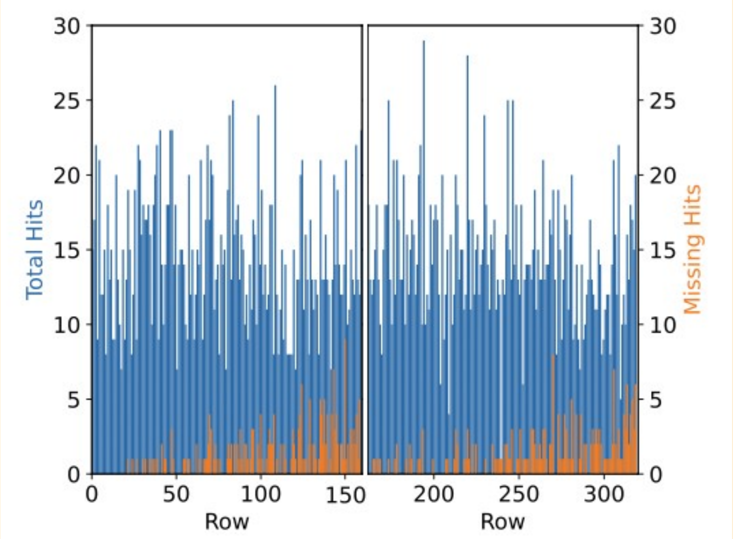
- For MightyPix2 the plan is to have two hitbuffers per column, this would increase the maximum hit rate by ~2

4x nominal hit rate (68 MHz)



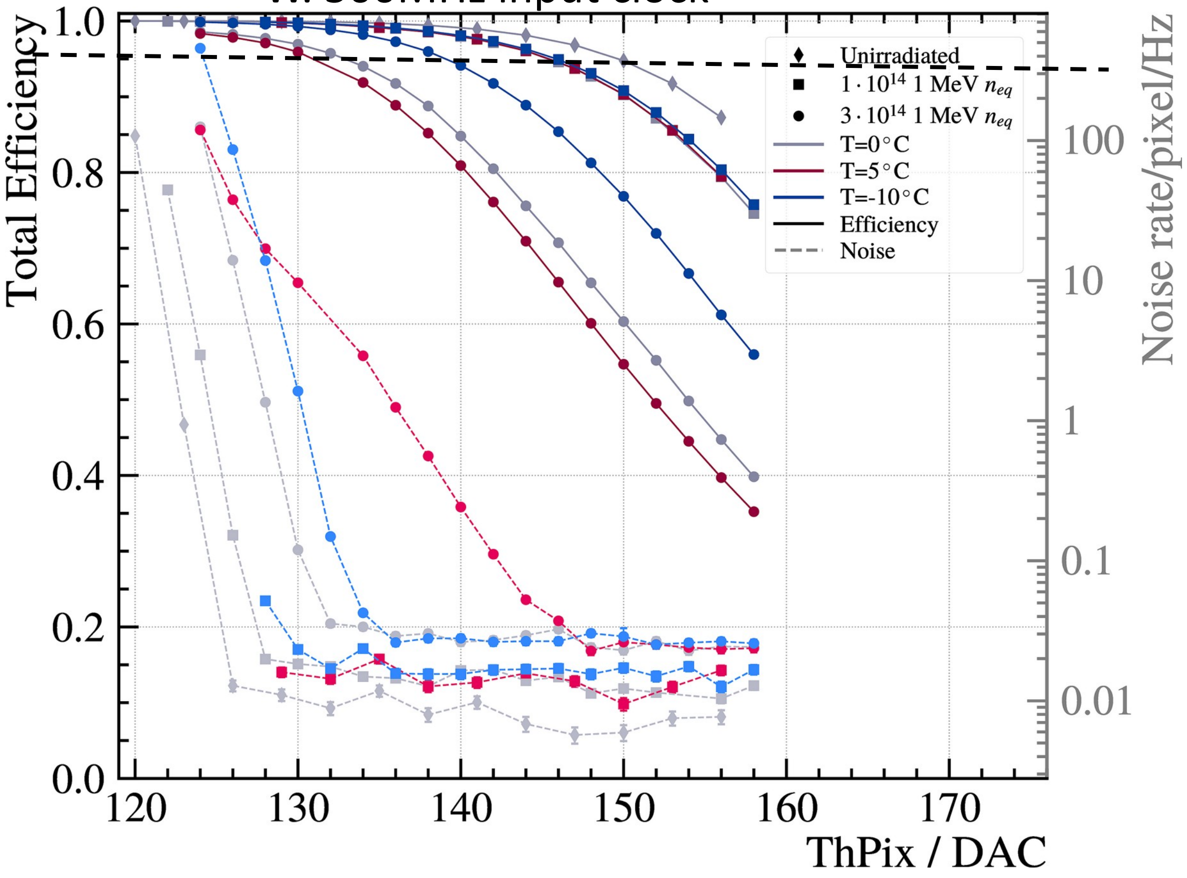
First simulation test 2 hitbuffers per row

Testbeam with AtlasPix3.1

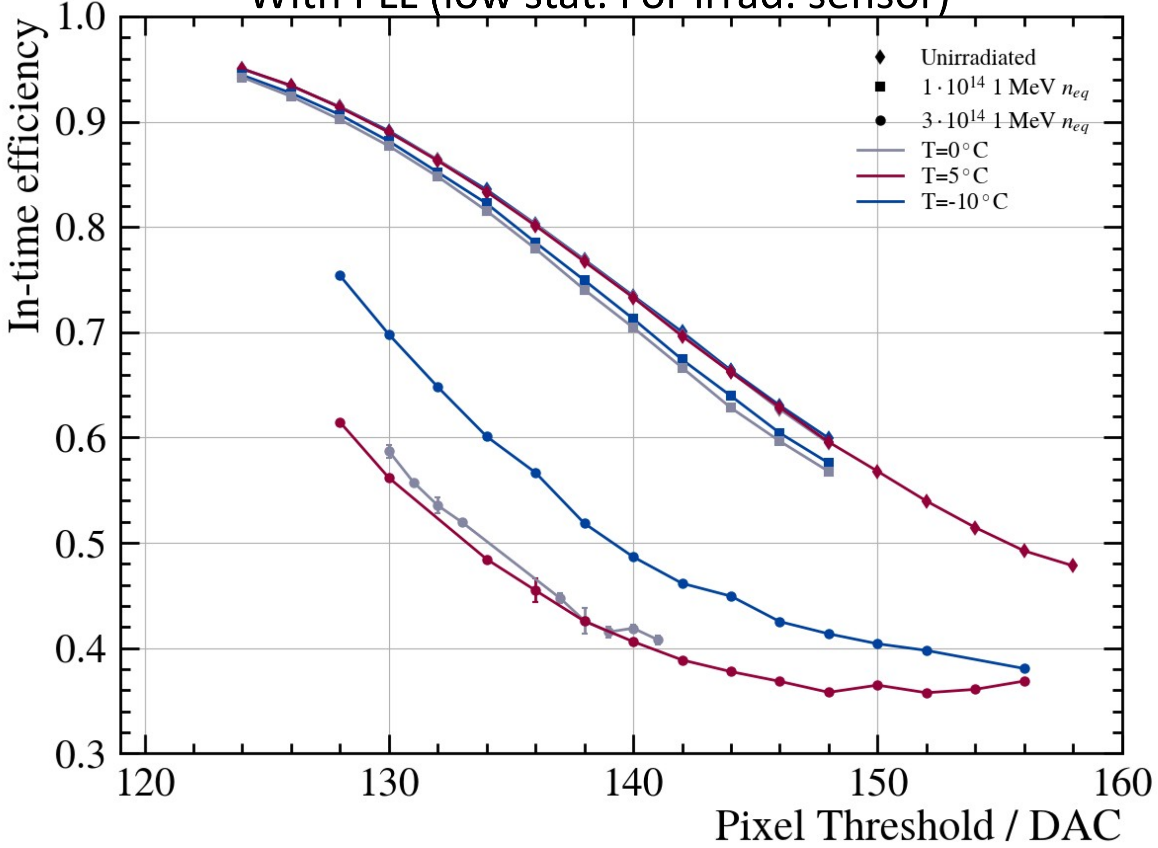
- AtlasPix3.1 is the closest full size chip of the HVCMOS family
- Amplifier and Comparator are different (no 3ns time resolution)
- Interest in the radiation hardness and stability of the time resolution

Testbeam results

Dec. 22:
W. 500MHz input clock



In-time efficiency=hit within 25ns
June 22:
With PLL (low stat. For irrad. sensor)



AP3.1 shows a short operation range

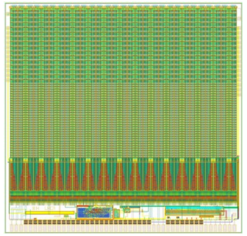
Significant decrease in efficiency at $3 \cdot 10^{14}$ MeV n_{eq}/cm^2

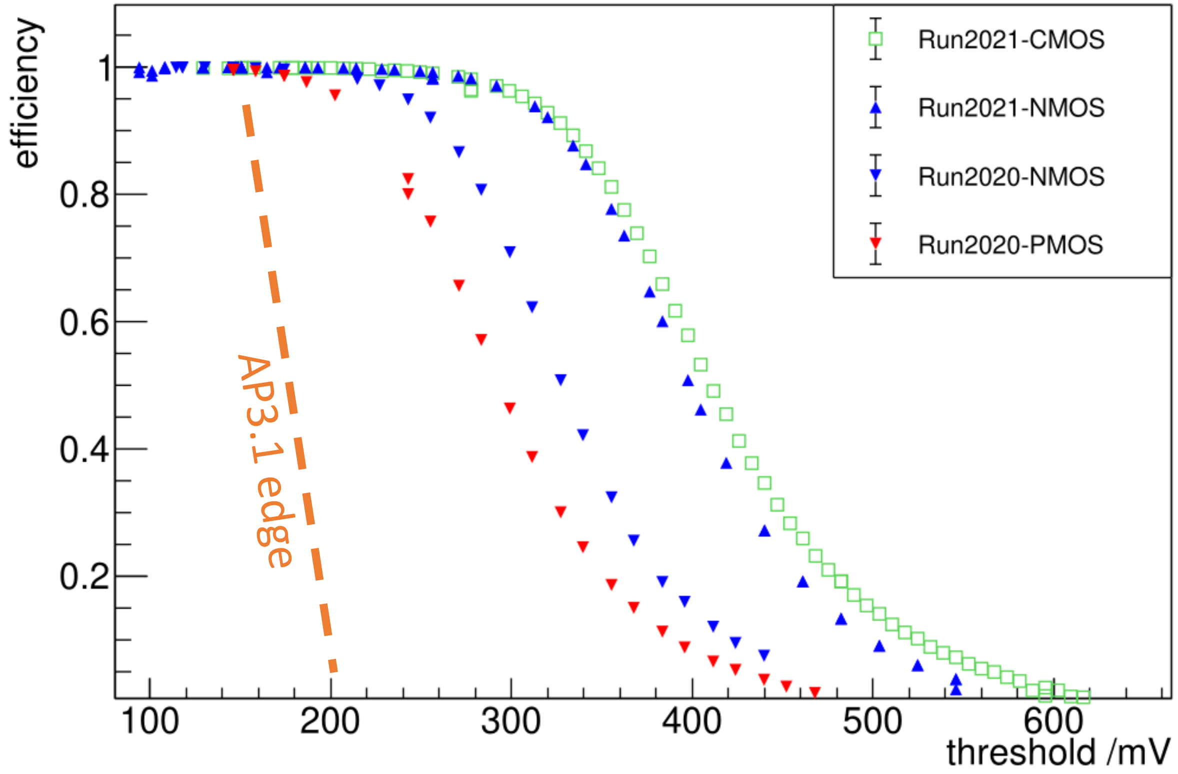
External clock (high frequency) recovers a bit the efficiency, but only with cooling some operation possible

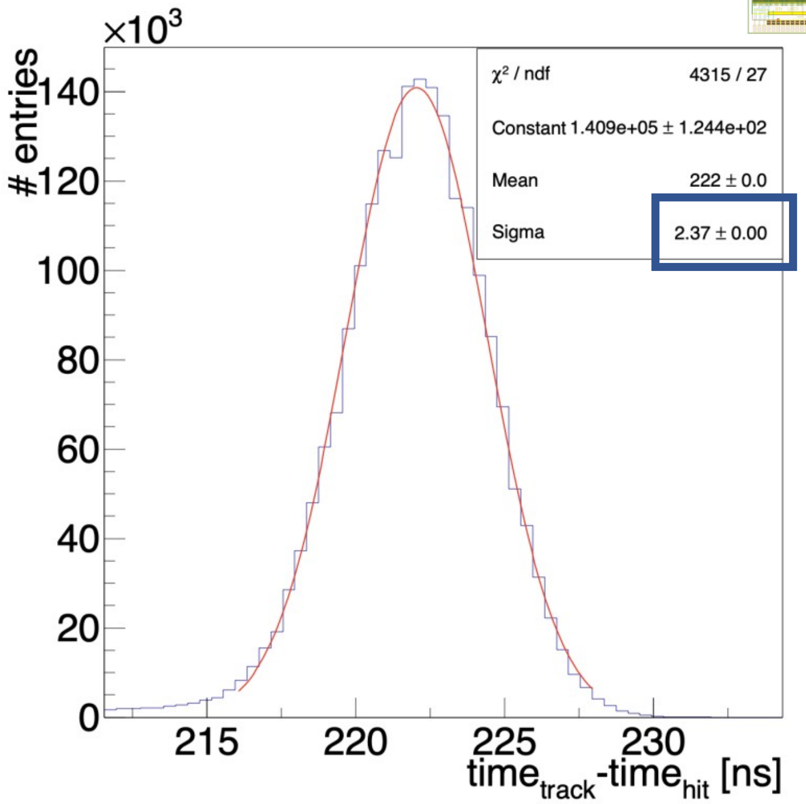
arXiv:2212.10248

Results for Run202X

Same analoge pixel as MightyPix1 (with half the size)
Different Periphery







This shows the good performance of the new amp and comp design.
The core Gaussian TOA distribution looks very good.
No tests with irradiated sensors

Summary of Current Results and Plans

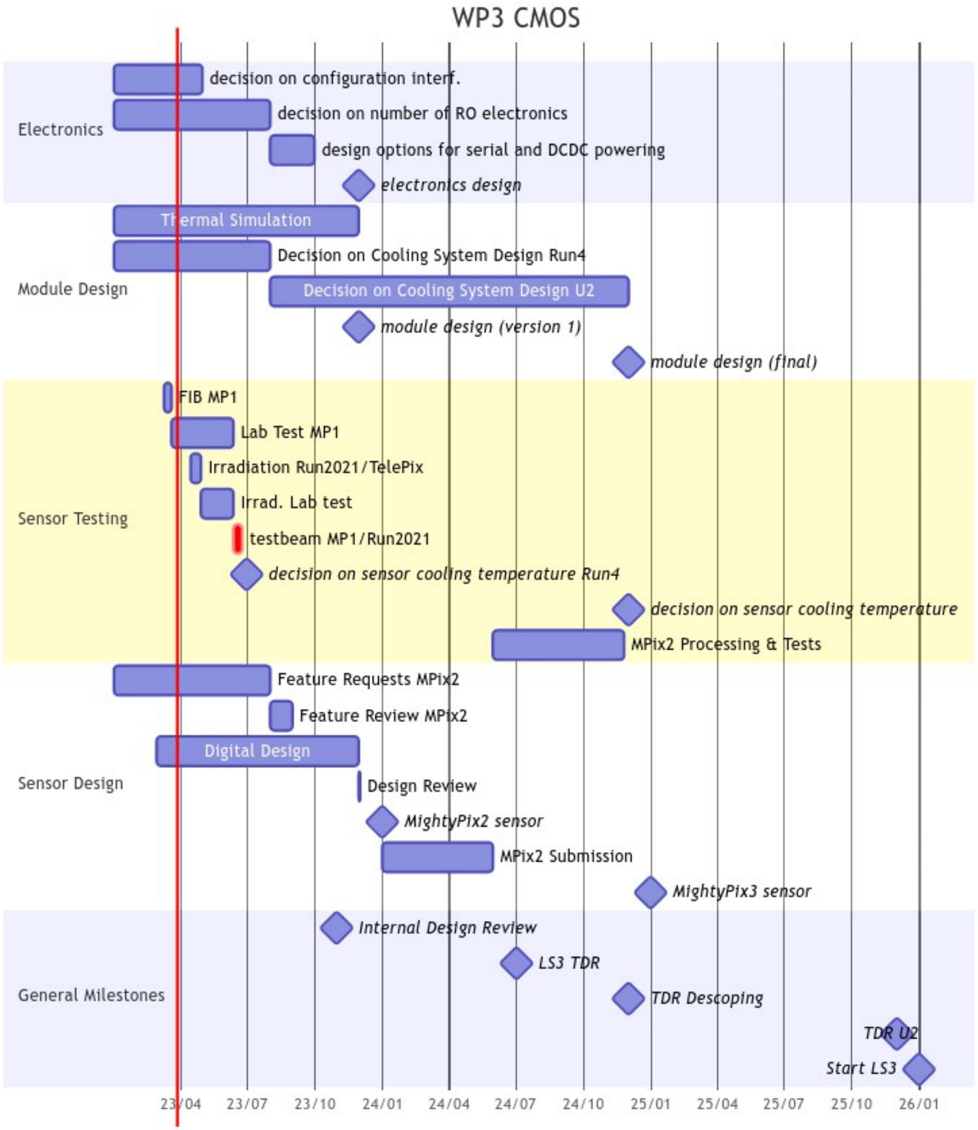
- Unirradiated AP3.1 has a wide enough high efficiency plateau
  - Timing as expected, but not enough for LHCb
  - Run2021v2/Telepix showed a high enough
- Rad. Hardness not as expected
  - Several ideas (Base substrate problem, some DACs might be not optimal...)
  - Initial plan to test this with MightyPix1 probably not enough chips
- Test FIB fixed MightyPix1 unirradiated
- Test Run2021v2/Telepix irradiated

Future and Planning

Known Unknowns:

- Operation Temperature
- Power delivery (DCDC vs serial/direct)
- Radiation Hardness
- Cooling

Plans:

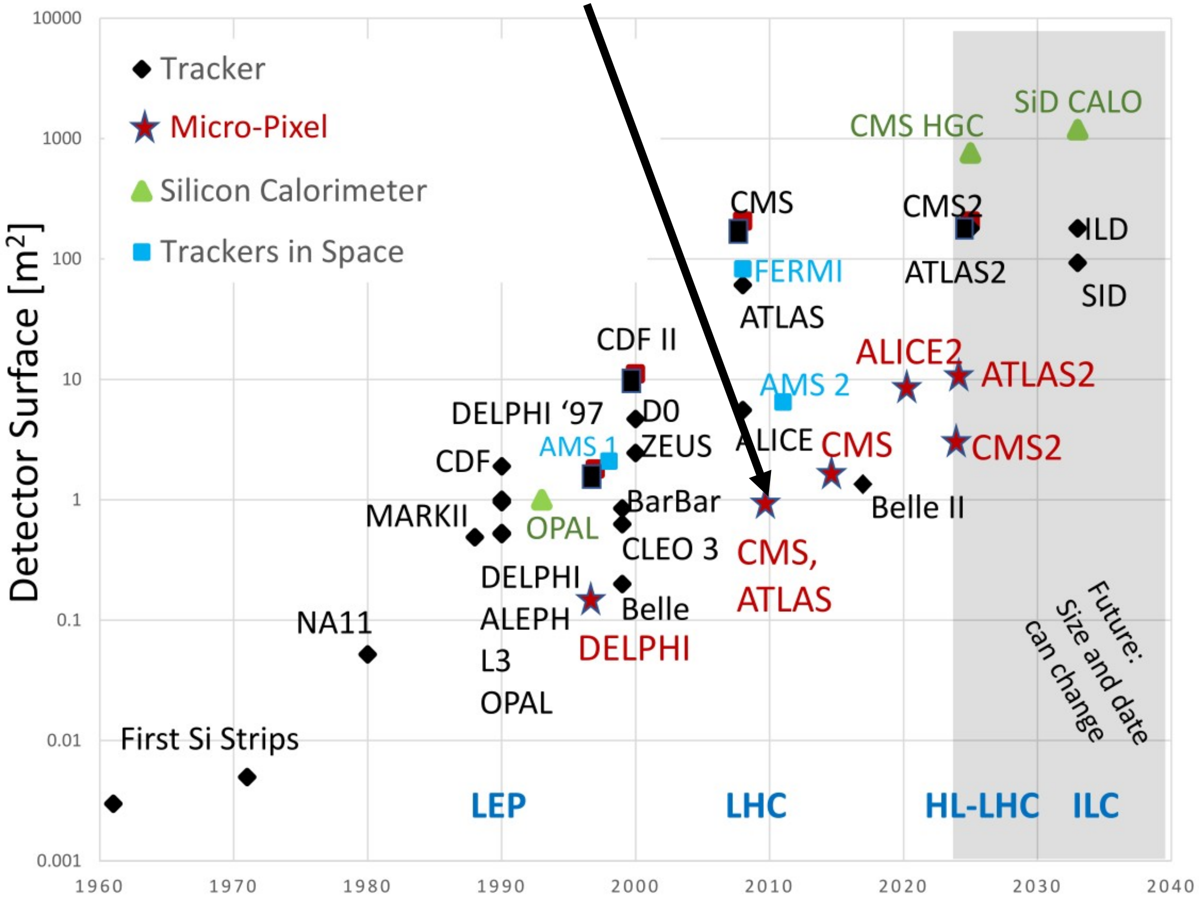


- Operation Temperature
  - Testbeam + Fixed MightyPix 1
- Power delivery (DCDC vs Serial/direct)
  - Do both designs
- Radiation Hardness
  - Testbeam
- Cooling
  - Have all the information to decide by the end of next year

LS3 detector (Path finder mission):

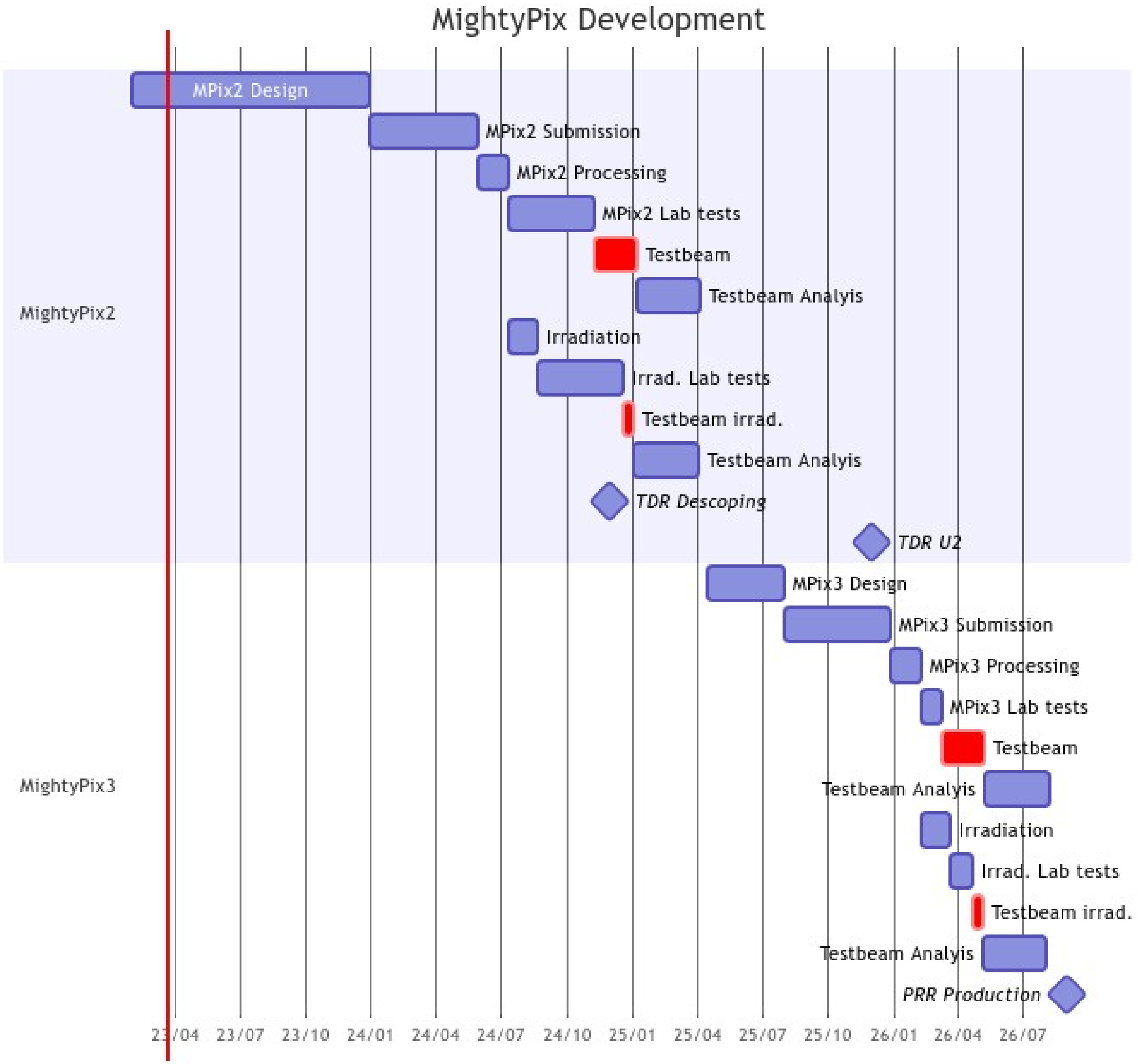
- LS3 is an important Milestone to have a flawless detector in U2
- physics improvements (is the condition)
- Smaller scale detector (decision based on simulation how big 1-2 Layers around the beampipe)
- Chip would be ready (with DCDC or direct powering)
- Cooling probably not below room temperature
- Independent Support from SciFi

Even if we build a $1m^2$ Detector



Plot from Frank Hartman
Pixel 2022/Evolution of Silicon Sensor Technology in Particle

MightyPix plans



For MightyPix2 (full sized chip) we leaned from MightyPix1
Long submission time of 6 month is not helping

The timeline for MightyPix2 and MightyPix3 (to be used in LS3) is tight

Summary

- A lot of work already done
- Module Design in last iterations
- Electrical DAQ layout being finalized
- Sensor is fast enough
- Radiation Hardness to be shown
- Lots of work until U2 still to do
- Internal System review planned for end of this year
- Plan of how to move forward clear

MightyTracker Workshop Bonn
31 May 2023 to 2 June 2023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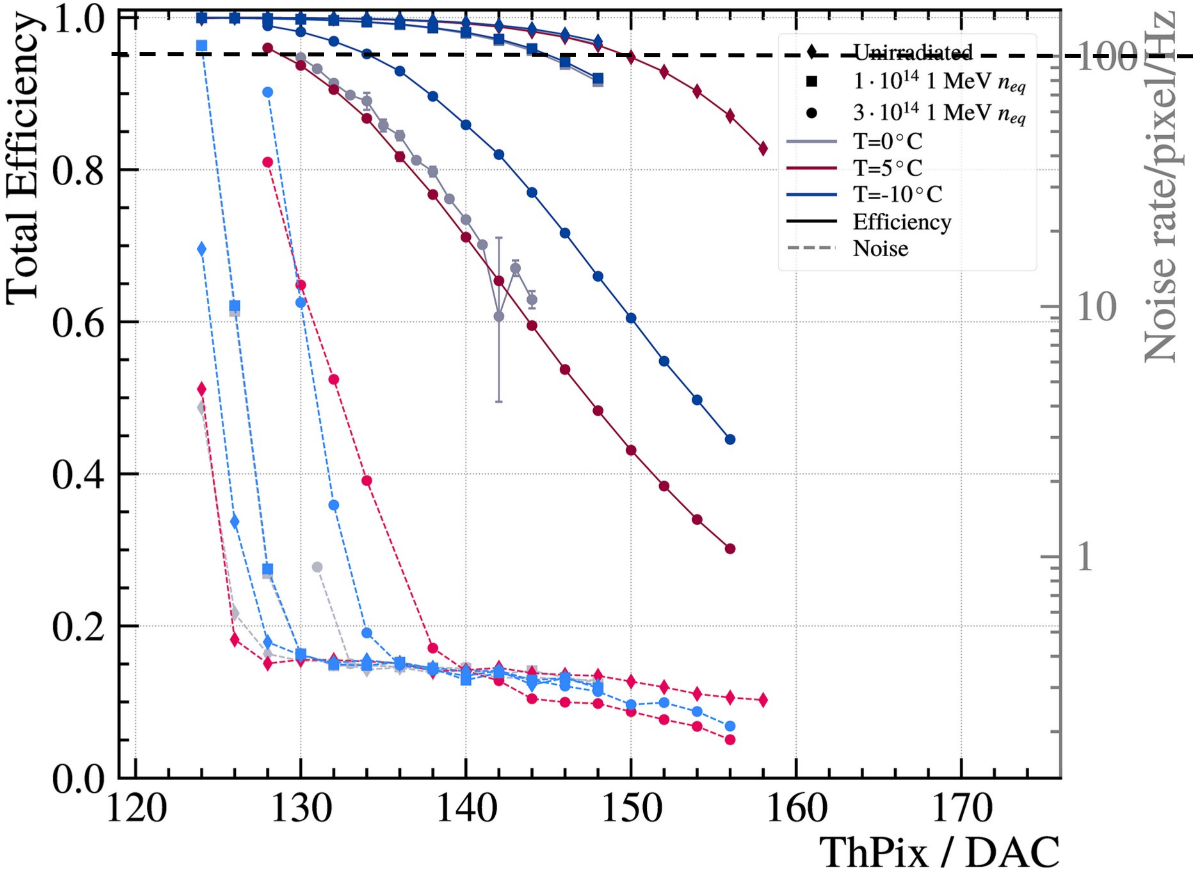
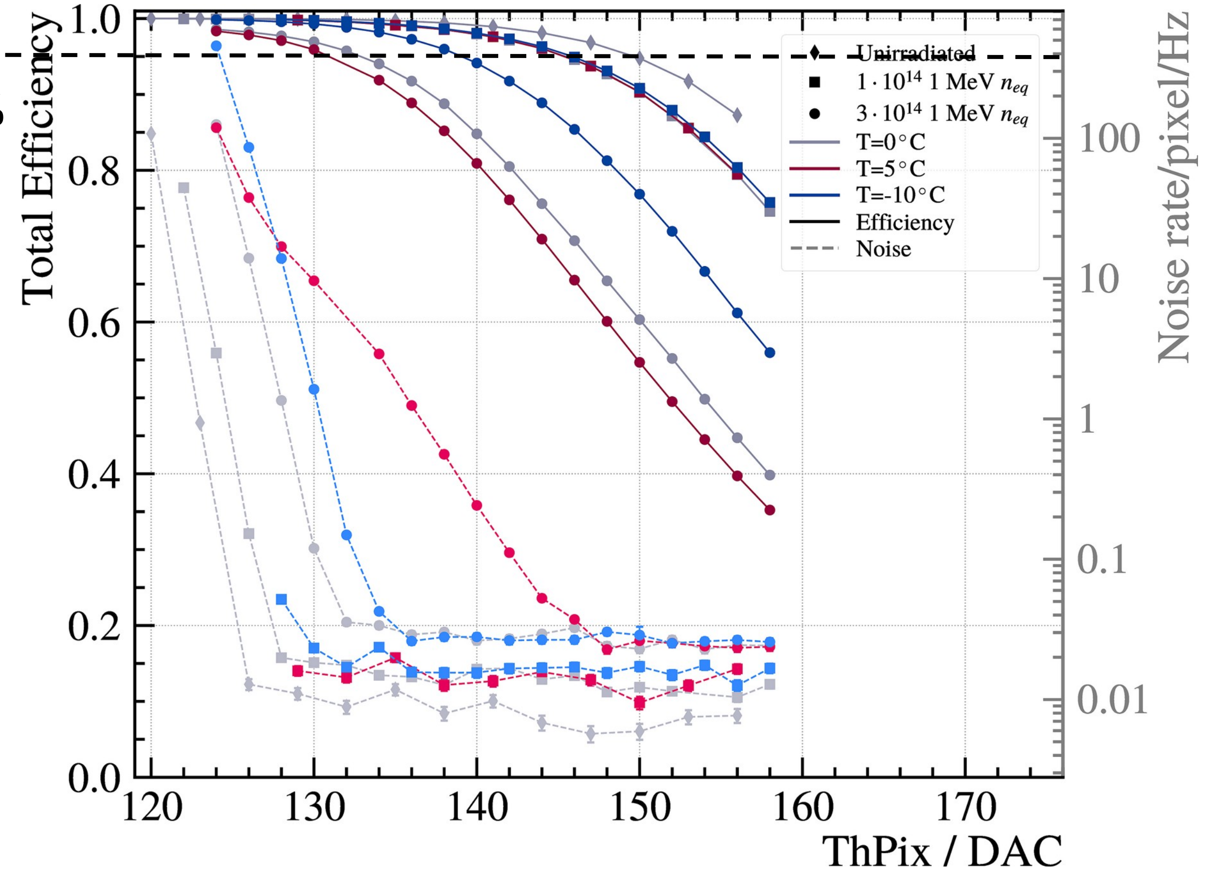
Backup

Testbeam results

June 22:
With PLL (low stat. For irrad. sensor)



Dec. 22:
W. 500MHz input clock



AP3.1 shows a short operation range

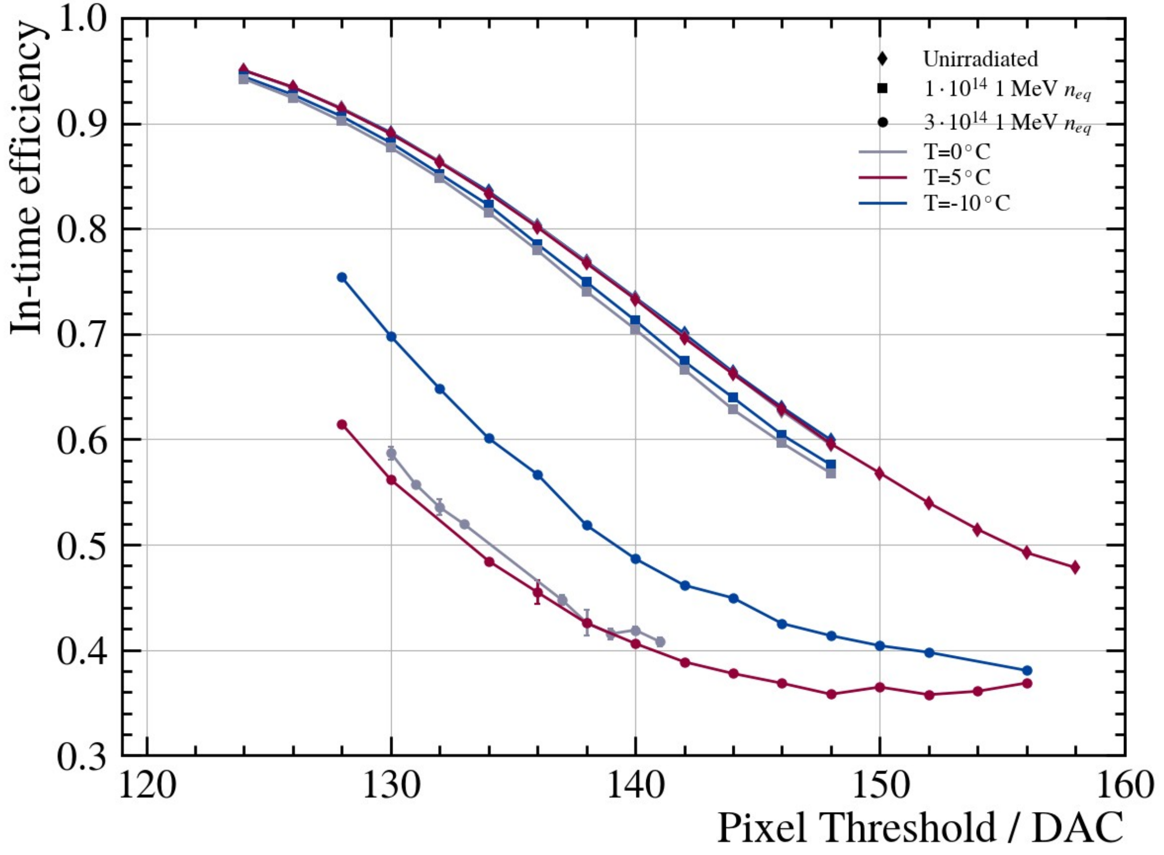
Significant decrease in efficiency at $3 \cdot 10^{14}$ MeV n_{eq}/cm^2

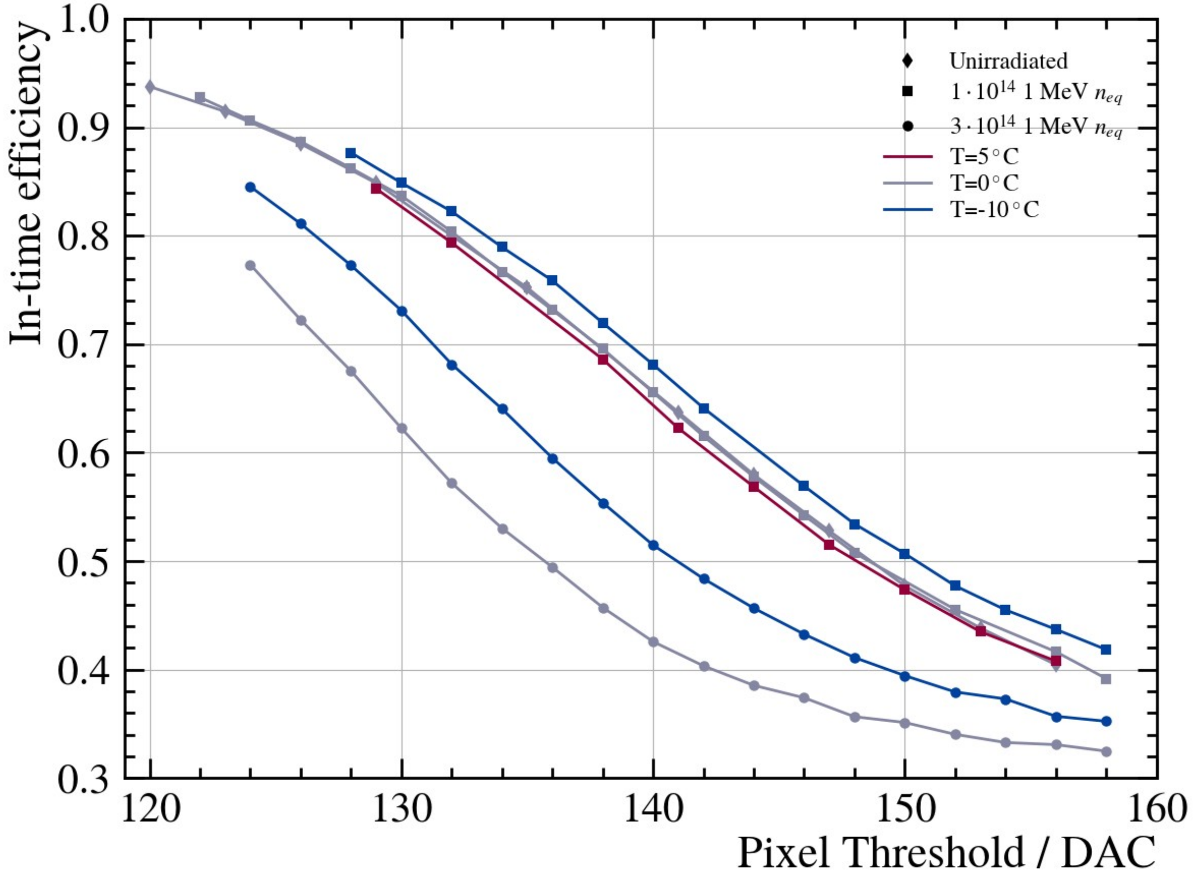
External clock (high frequency) recovers a bit the efficiency, but only with cooling some operation possible

This is with TOT and row correction

In-time efficiency=hit within 25ns

Timing

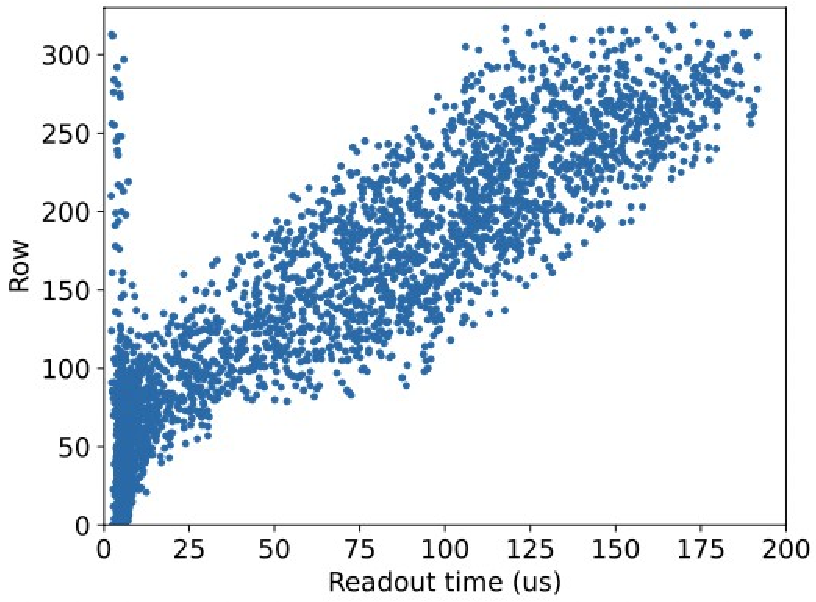




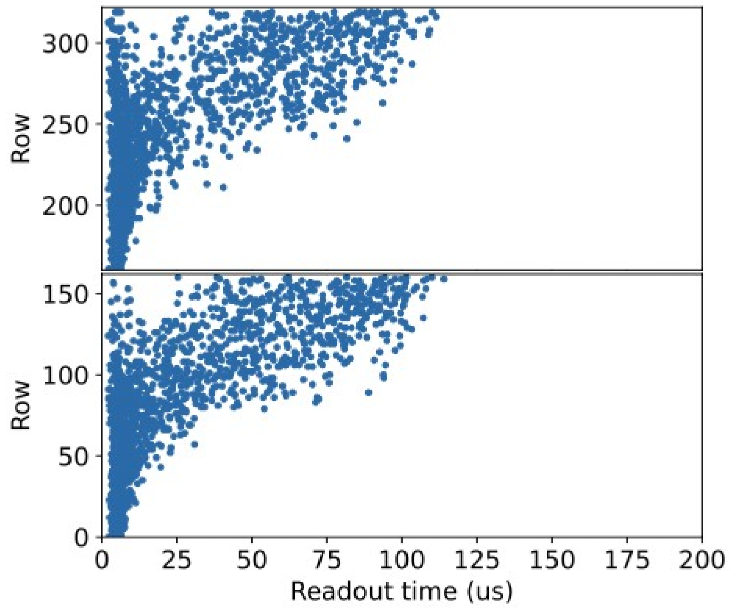
As expected the time resolution is not good enough (~5ns at best)

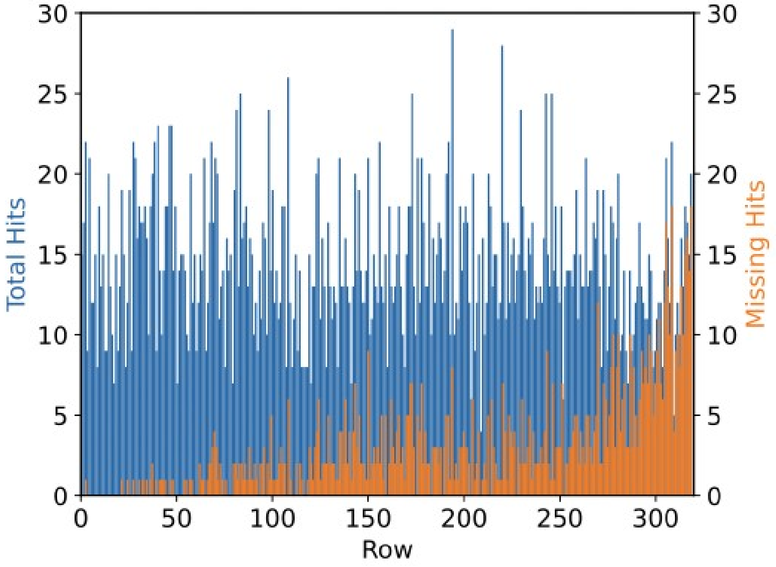
High impact of the radiation for $3 \cdot 10^{14}$ MeV n_{eq}/cm^2

Hit Rates

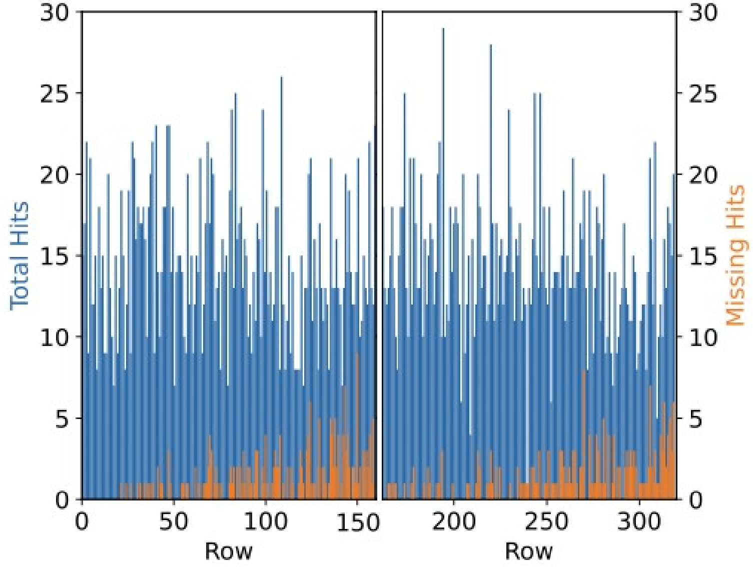


Increase
number of
End of Columns
(EoC)

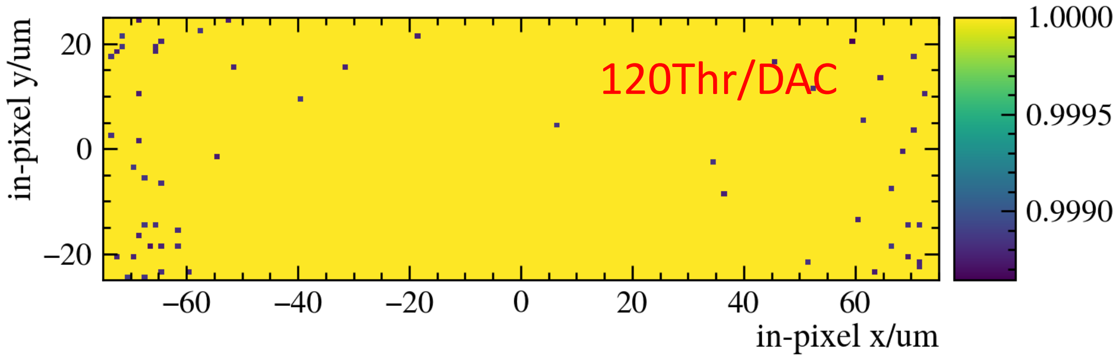


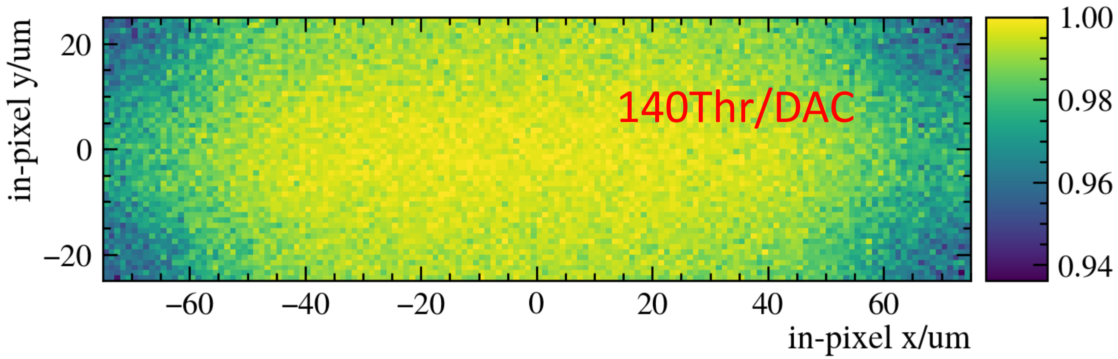


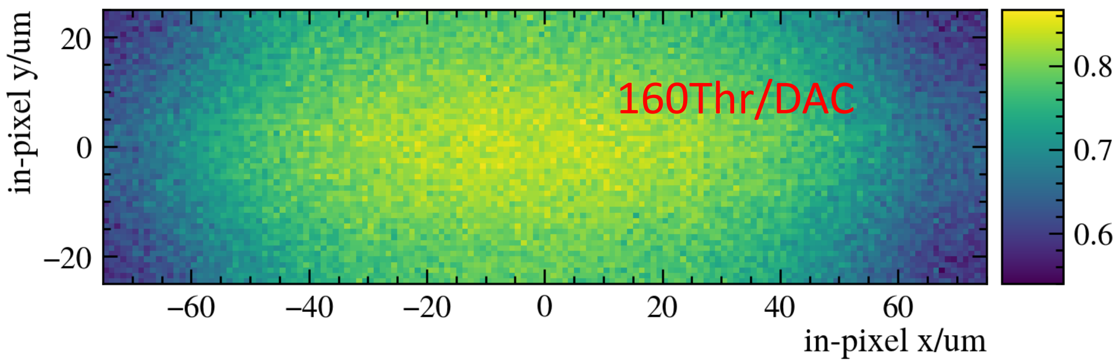
Increase
number of
End of Columns
(EoC)



Single pixel Efficiency





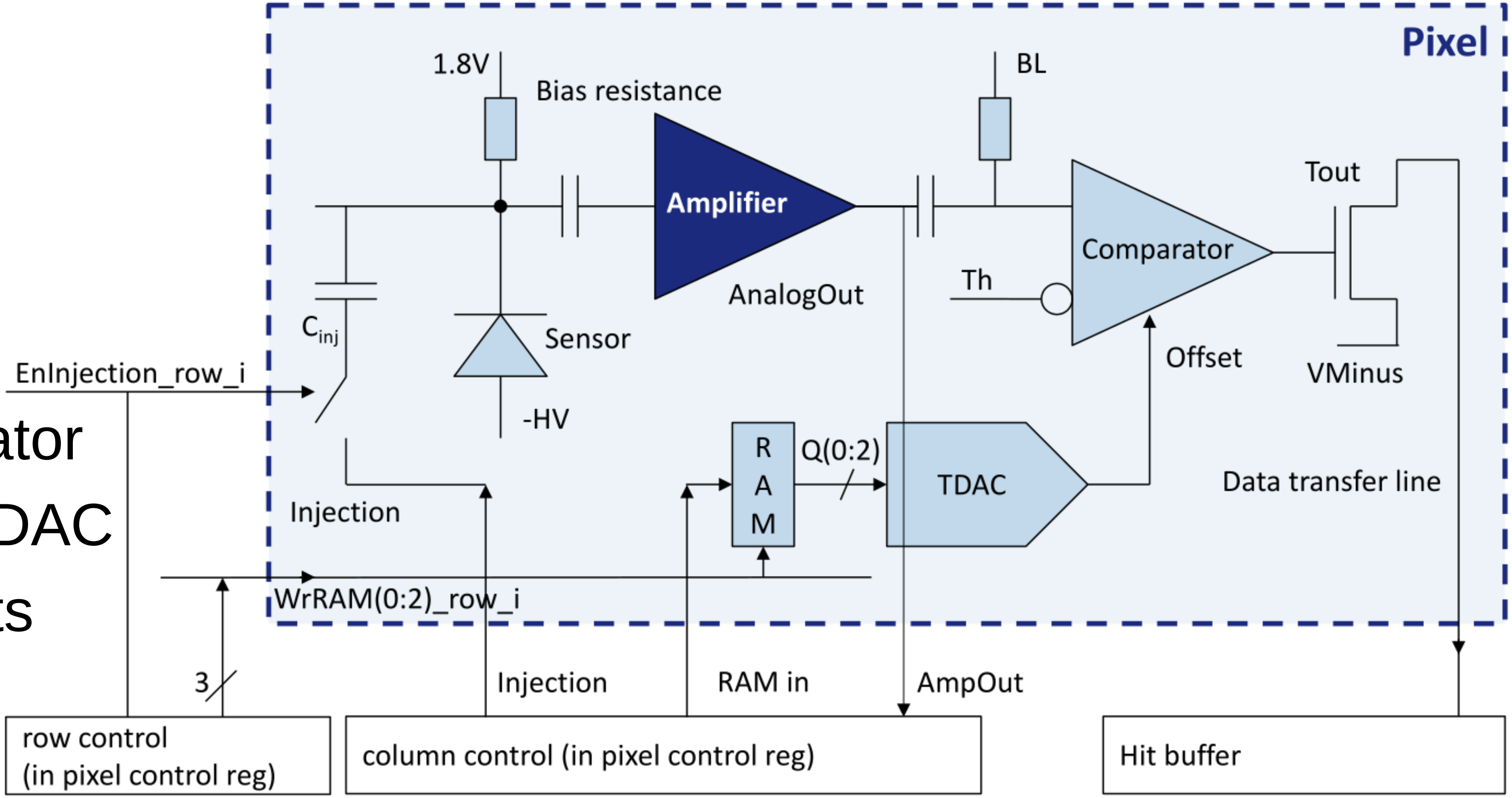


- Overlay of all pixels
- As expected first loosing the corners
- We know that a higher bias would compensate this (partially)
- Corners and short side loose the most charge due to charge shearing with neighboring pixels

Analogue Part

In Pixel:

- Sensor diode
- CSA amplifier
- CMOS Comparator
- Threshold tune DAC
- RAM for tune bits



Source: Ivan Perić

Proxy

	AP3.1	Run2021 V2	Run2021 v3	MP1 fixed
Hit Rate	Done	✓ (orange)	✓ (orange)	✗
Timing	Done	✓ (orange)	✗	✗
Rad. Hard.	Done	✓ (orange)	✓ (orange)	✗
Power	✗	✗	✗	✓ (green)
Energy response	✗	✓ (orange)	✗	✗

A few things can be checked with other chips, but none is an exact match.

Main problems are:

TFC
CMOS PLL

We will not be able to perform rad. Tests with the fixed sensors.

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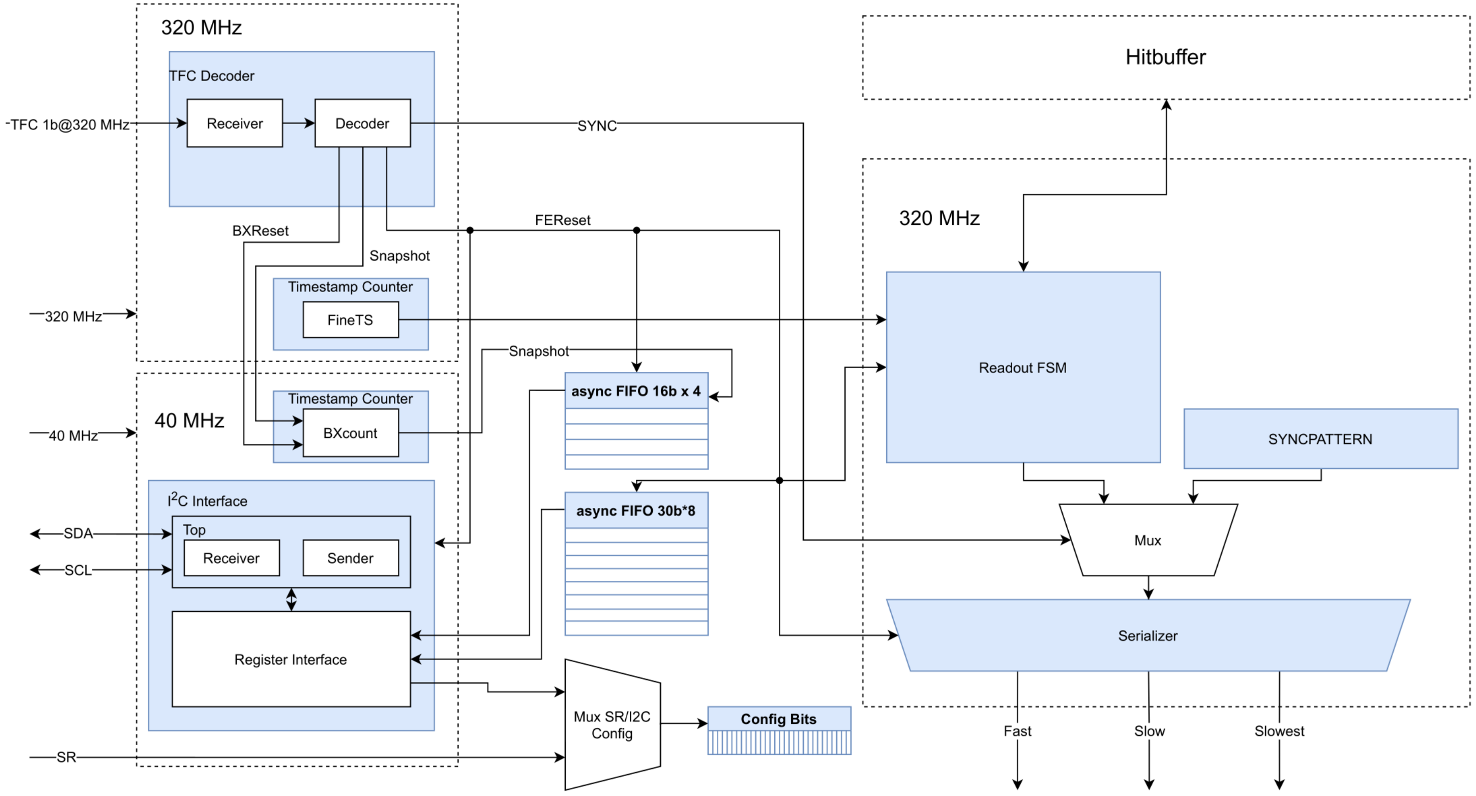
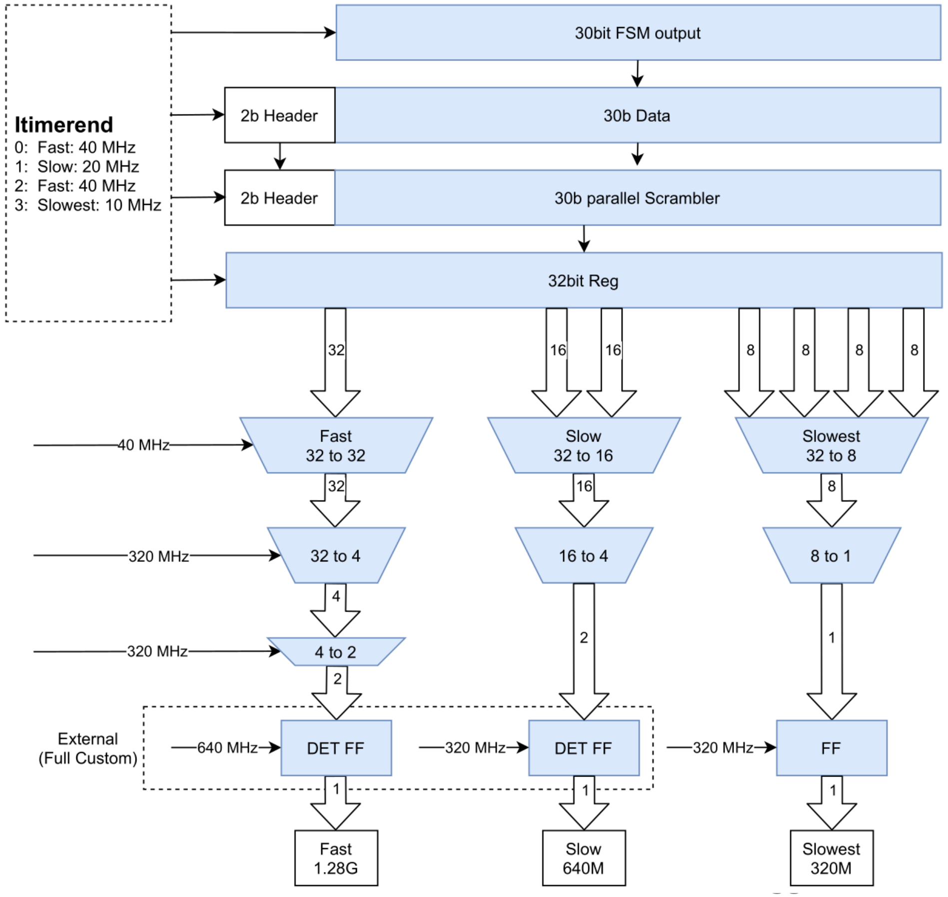
Current Electronics Estimations

LHCb Mighty Tracker - Silicon only (monolithic CMOS sensor chip)																
	Long sub-module	Long module	Short sub-module	Short module (!)	Inner Tracker (one layer), LS3 only		Inner Tracker (three layers), LS3 only		IT only, LS3 only	IT only, LS3 only	Middle Tracker (one layer)	Middle Tracker (six layers)	Middle Tracker (six layers)	IT only, UGII	UGII (six layers)	Mighty Tracker
	Single-sided	Double-sided	Single-sided	Double-sided	Long modules (4)	Short modules (2)	Long modules (4)	Short modules (2)	No spares, no R&D	w/ 10% spares, 10% R&D	Long modules (22)	Long modules (22)	w/ 10% spares, 10% R&D	w/ 10% spares, 10% R&D	IT + MT	Total = LS3 + UGII
Mighty Pix chips	35	280	20	220	1120	440	3360	1320	4680	5616	6160	36960	44352	11232	55584	66816
lpGBT	"3-5"	"24-40"	"2-6"	"20-44"	96	40	288	120	408	489,6	528	3168	3801,6	1497,6	5299,2	6796,8
VTRX+	"1-2"	"8-16"	"1-2"	"8-16"	32	16	96	48	144	172,8	176	1056	1267,2	518,4	1785,6	2304
DCDC bPOL12V	5	40	3	32	160	64	480	192	672	806,4	880	5280	6336	1612,8	7948,8	9561,6
linPOL	"2-4"		"2-4"		64	32	192	96	288	345,6	352	2112	2534,4	1036,8	3571,2	4608

https://docs.google.com/spreadsheets/d/1ZYi1KfIiTQx_eC8736JTl1Mz8Gj5eVcB76Z9e5rynao/edit#gid=0

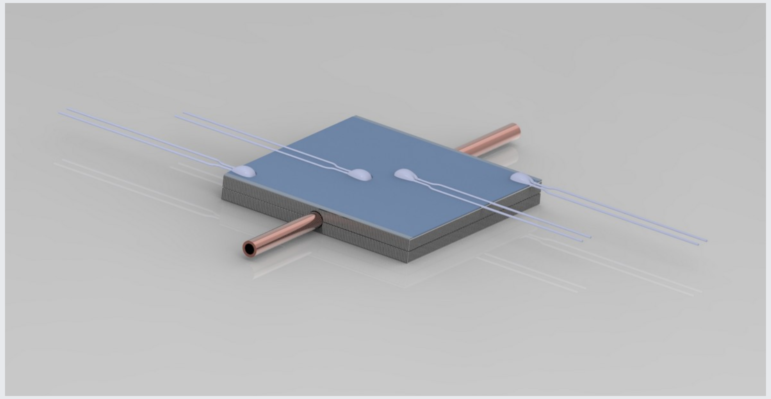
FSM and Serializer





Design vs. Initial Specification

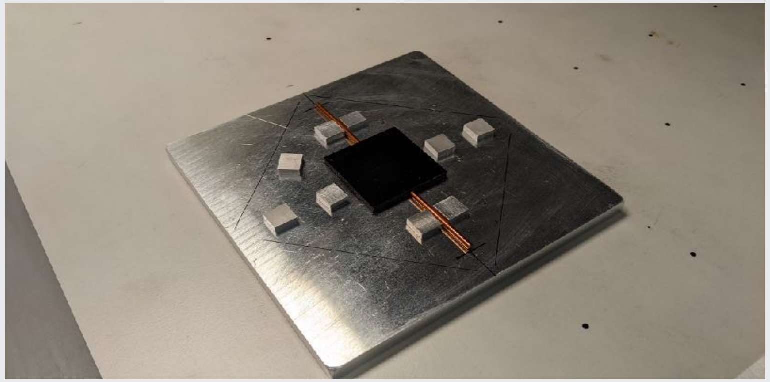
- Smaller Pixels -> 55 x 165 μm^2
  - Time Resolution
- No negative impact expected (zero suppressed)
- Adjustable clock frequency (reduce the number of lpGBTs)
- For the future:
  - Faster (differential) configuration
  - Improved TFC compatibility
  - Provide external 2.5V input (to be converted to 1.8V internally)
  - Serial Powering



Dimensions 40mm x 40mm x 4.1mm

Assembly Contains:

- 2x half Carbon Foam layers
- 1x Cooling Tube
- 2x Carbon Fibre Sheets
- 4x Dummy Silicon Chips
- 1x Silicon El.Heater
- 4x NTC Thermistors

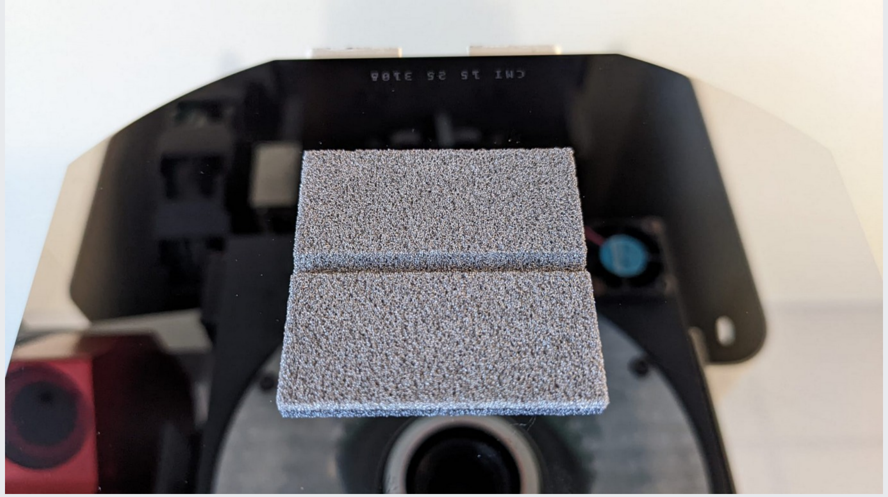


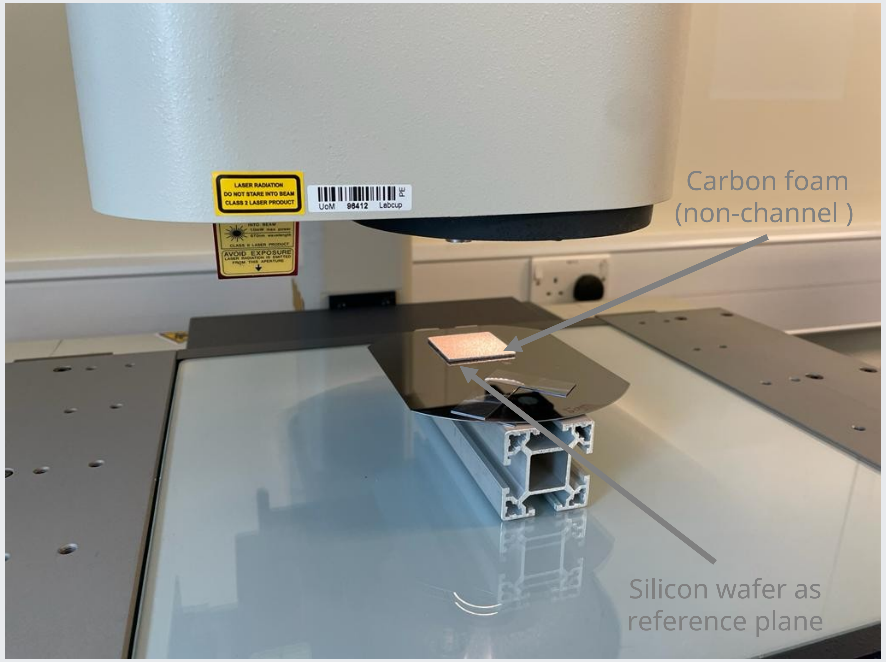
1. Mechanical Prototype:

- Foam Cleanings
- Foam Cutting Tolerances
- Cooling Channel Cutting
- Glue Choice (ARALDITE® / LOCTITE STYCAST / ...)
- Gluing Procedures / Patterns
- Gluing “Veils“
- Silicon Chip handling (Pick & Place)
- ...

2. Thermal Prototype

- Thermal FEA
- Thermal Figure Of Merit
- Heat Load (El.Heater)
- Cooling Performance
- Different Thickness of material
- Different tube OD /ID
- ...





Metrology is done using the **OPG Smartscope Flash 500**

We have machined 12 samples (3 broke):

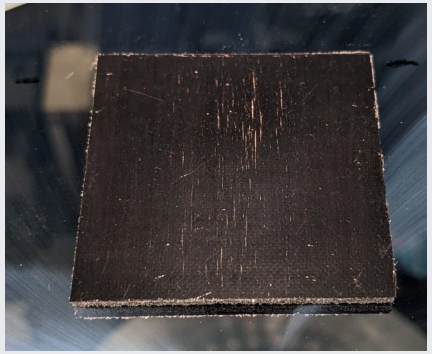
- 40 x 40 mm^2 , 2 mm thick, C-Foam layers with cooling channel

- Foam is from Lockheed Martin ©, standard density (0.2 - 0.26 g/cm^3)

- Co-cured with 150μ thick carbon fibre sheets at Liverpool University

- Carbon fibre sheets: 3 layers of carbon fibres, in 0-90-0 orientation

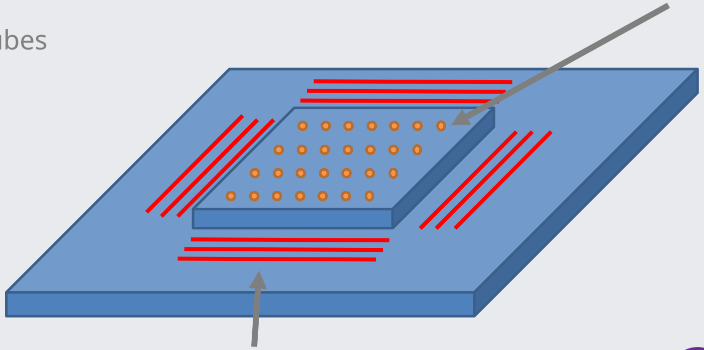
- 4 samples done with “0” layers oriented along cooling channel and 4 with “0” layers oriented perpendicular to cooling channel



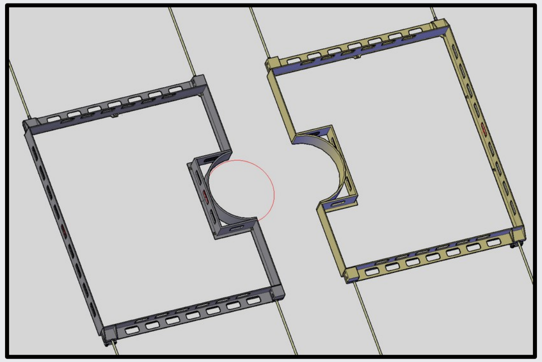
Co-cured Sample

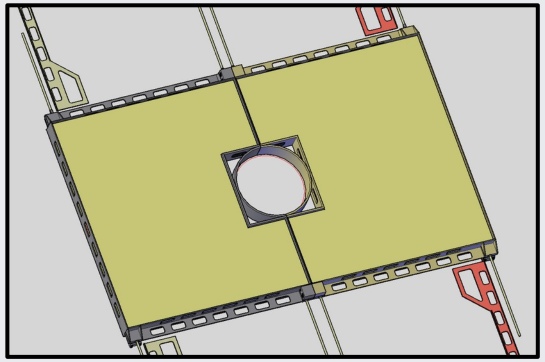
Work done:

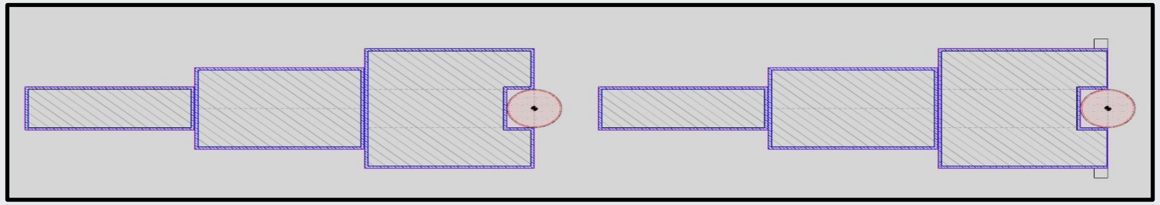
- Do the metrology and compare with pre-co-curing results
- Find best technique for metrology
- Check all 8 samples
- Assemble “sandwich” with polyimide tubes
- Perform cooling studies

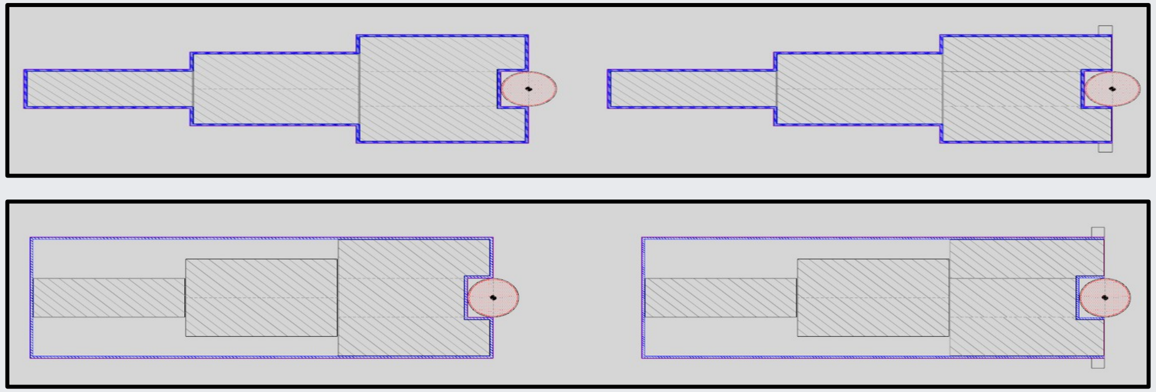


- ✓ Carbon Fibre support structure (frame) design - discussed the different design options.
- ✓ Material for this support frame - the Radiation resistance properties and the contribution to the overall material budget.
- ✓ Installation (extraction) sequence - Two options (directional) are under the consideration. Front side mounting or sideway sliding.
- ✓ Vibrations that are (could be) caused by the sliding/mounting of the modules.
- ✓ Module planarity pins (special fiducials/locators with higher precision) to ensure the module planarity within the frame.
- ✓ Cooling pipe interconnection between the modules - We design special connection points /connectors to ensure the removability of the modules and the workability of the cooling lines (and the modules).
- ✓ Service (cables/pipes) distribution - Vertical (Top and Bottom). Horizontal distribution is not favourable.
- ✓ We need to well understand and discuss with the SciFi team installation instruments and the sequence.
- ✓ We need to well understand and discuss with the SciFi team the space (support surface) for the MT module frame and its supporting structure. Both Bottom and top locations.









Integration into the SciFi :

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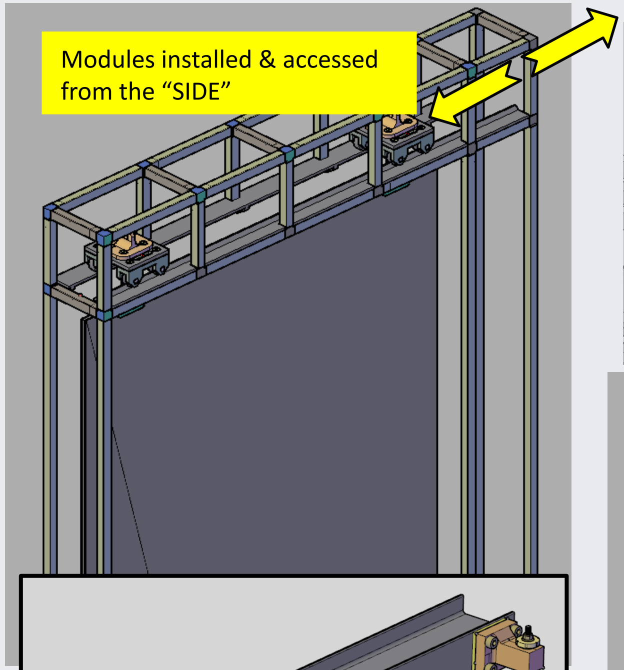

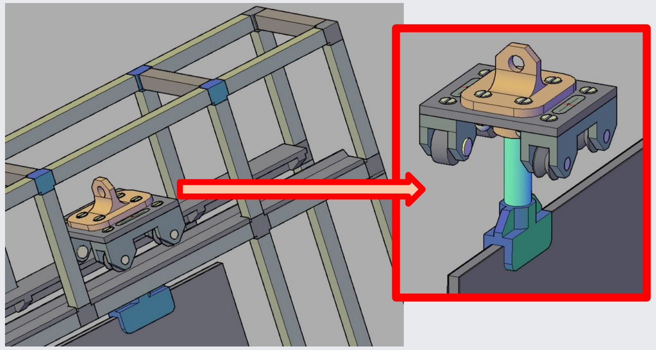

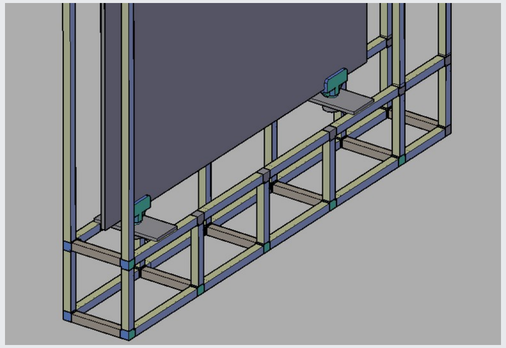

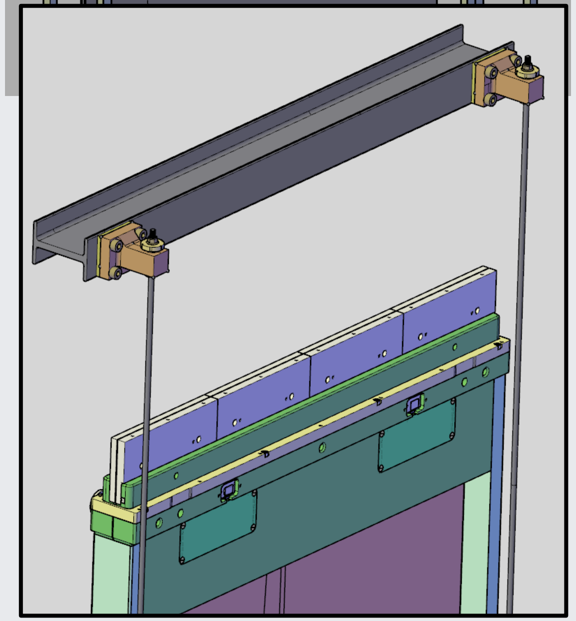

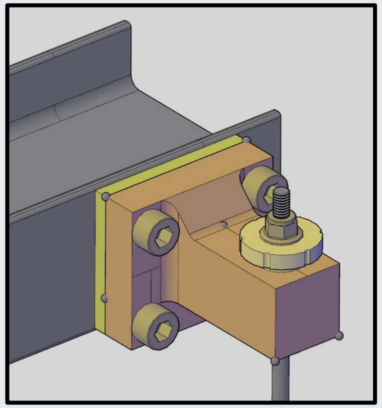

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