MAPS-based UT for LHCb Upgrade II

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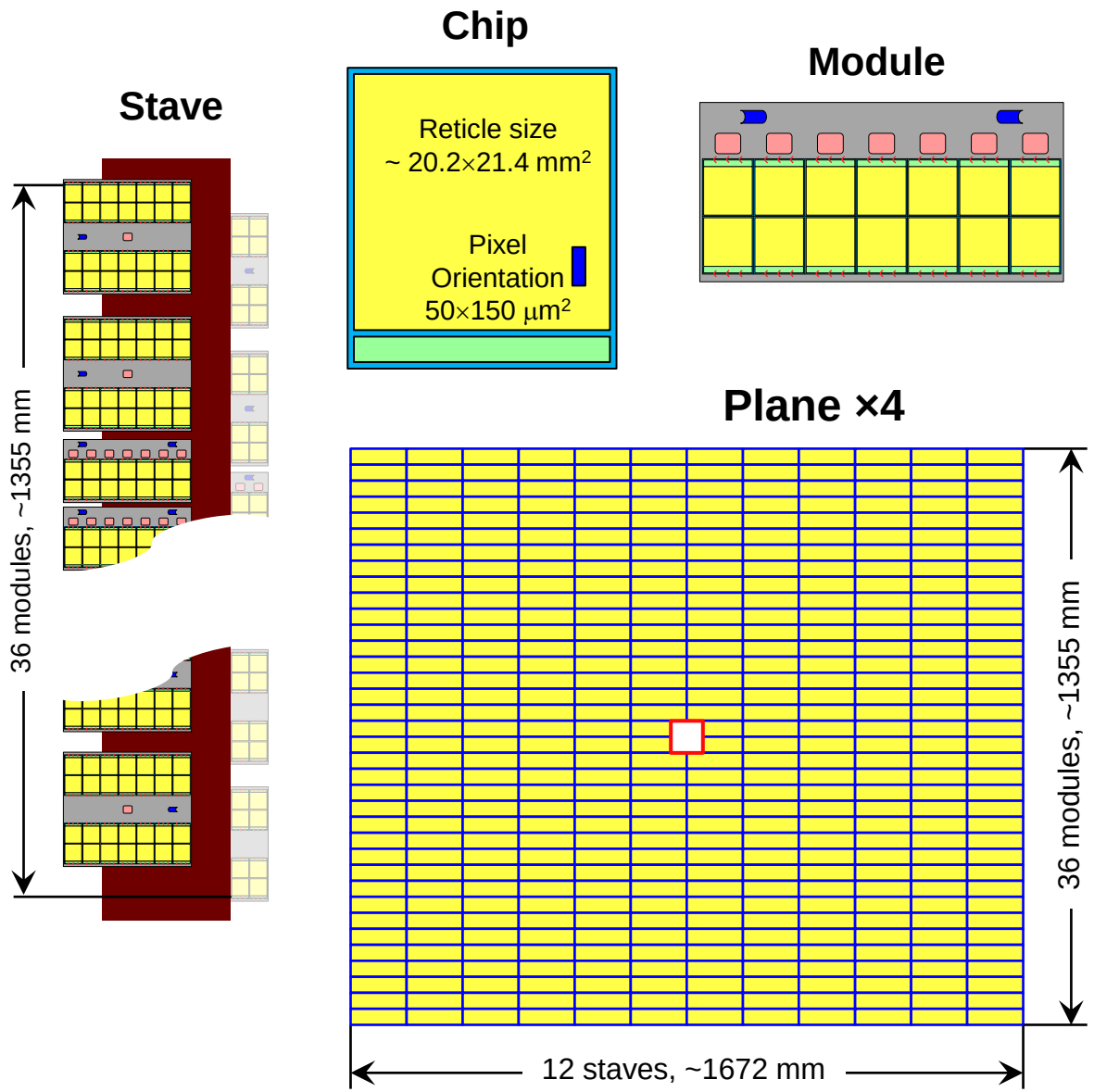
For the U2UT group

The 6th workshop on LHCb Upgrade II, Mar 29-31, 2023, Barcelona

Reminder: U2UT in FTDR



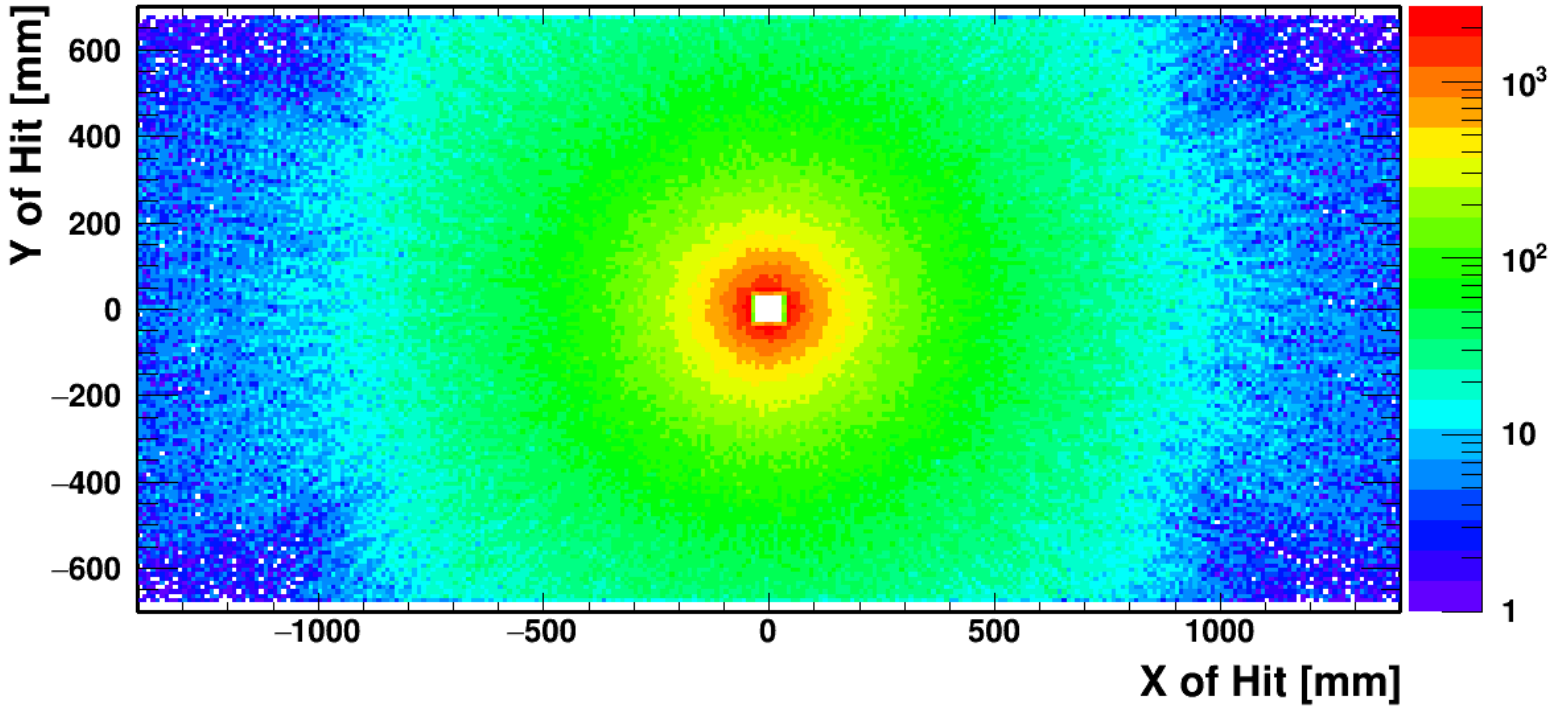
- The current UT can not be kept for U2.
  - Much increased track density requires higher granularity, especially in the central area.
  - Bandwidth for high data rate
  - Radiation hardness
- A MAPS-based pixel detector
  - Small electrode: MALTA
  - Large electrode (HV-CMOS): AtlasPix, MightyPix, …
  - Other technologies are not excluded
- Certain features of the current UT may be kept, e.g. the stave structure, and strip / long pixel orientation.

U2UT R&D Activities

- The FTDR is a good starting point. Much intense R&D efforts are needed.
- We report here progresses of selected activities:
  1) Detection coverage and de-scoping scenarios,
  2) Detector modelling and description, detector element coding, and radiation length,
  3) Tests of small electrode CMOS chip – MALTA2,
  4) Tests of large electrode CMOS chip – ATLASPix3,
  5) Attempts for alternative foundries, and with smaller feature size.

Study of UT Coverage and De-scoping Scenario

- The simulation and reconstruction software is not fully ready yet. Thus performance related to precision of track momentum can not be easily assessed yet.
- Require track to have ≥3 UT hits ⇒ compare scenarios of 4- & 3-planes.
- Adjust the horizontal coverage ⇒ impact on the reconstruction efficiency.

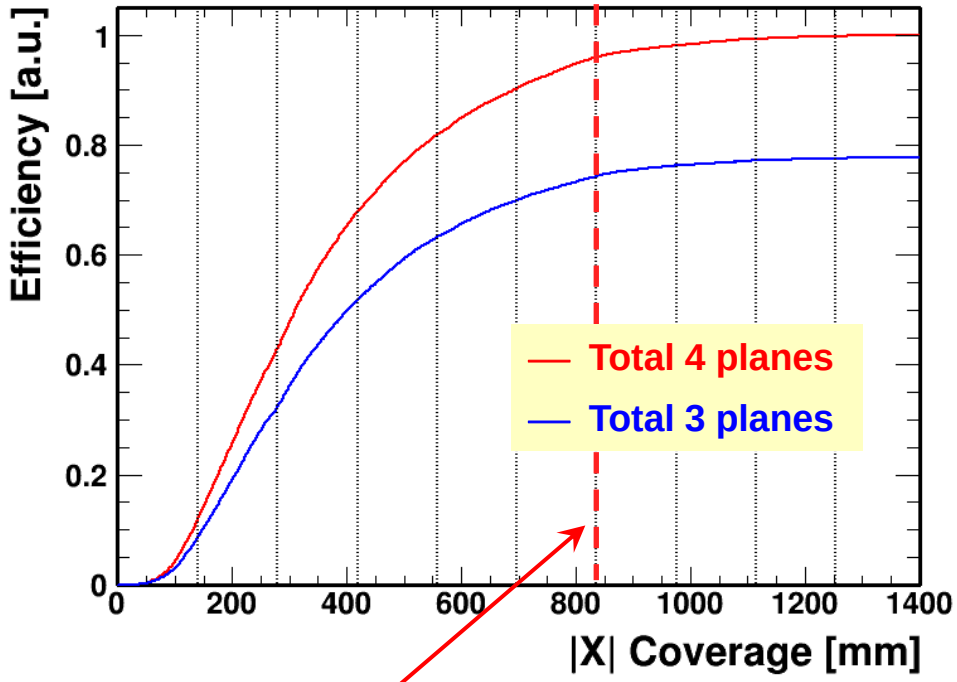


The FTDR design with wider planes
|X| < 836 → 1400 mm

Efficiency vs X Coverage and Number of Planes

$\overline{B^0} \to D^{*+}\pi^-, D^{*+} \to D^0\pi^+, D^0 \to K_s\pi^+\pi^-, K_s \to \pi^+\pi^-$

≥ 3 UT hits / track



- Coverage in Y: ±677 mm
- Beam hole: (±39.4) × (±37.1) mm^2
- Sufficient overlaps between ladders and modules
- Inefficient gaps between chips within each module
- VP, FT+MS are taken into account

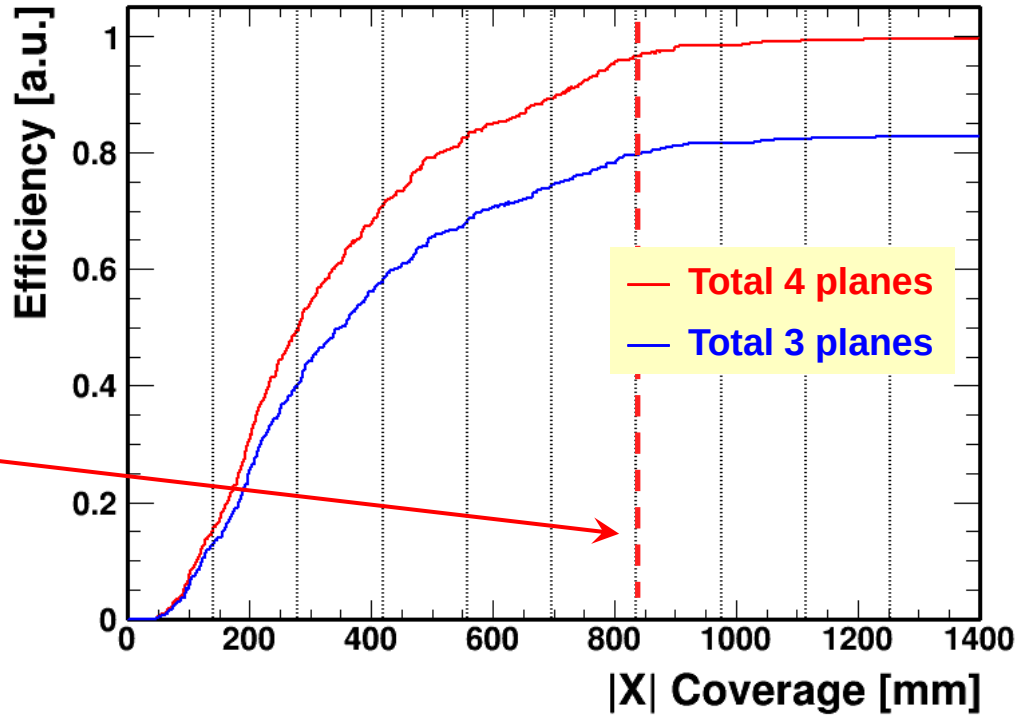
12 staves / plane |X| < 836.2 mm	Decay Chain	Single π from			
		B	D*	D	K_s
Total 4 planes	96.0	98.5%	99.9%	99.4%	99.5%
Total 3 planes	74.3	94.1%	95.8%	95.1%	95.4%

Efficiency vs X Coverage and Number of Planes

$$B^- \to D^0 K^-, D^0 \to K_s \pi^+ \pi^-, K_s \to \pi^+ \pi^-$$

≥ 3 UT hits / track

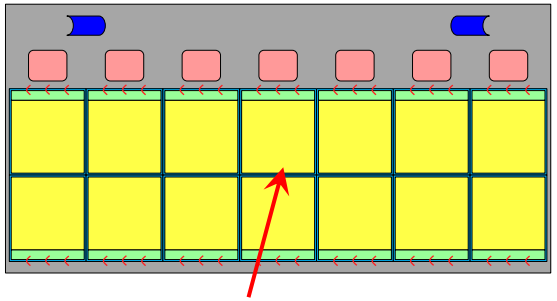
12 staves / plane |X| < 836.2 mm	Decay Chain	Single π / K from		
		B	D	K_s
Total 4 planes	96.5	98.5%	99.4%	99.6%
Total 3 planes	79.6	92.6%	96.0%	96.5%



Mini Summary and Thoughts

- Horizontal coverage
  - |X| < 836.2 mm with 12 staves / plane in FTDR is reasonable.
  - The value was based on the already optimized system, taking into account the new MS.
- Scenarios of 4-plane vs 3-plane:
  - The performance is significantly compromised with the 3-plane solution, especially for physics with multiple final state particles.
  - Size of individual pixel chip is limited by technology. It is difficult to reduce the inefficient area between chips.
  - A 200 μm gap is already very challenging. Inefficiency in the sensitive area is not included yet, and would enhance this trend.
  - Also descoping of UT has little impact on the overall budget.
- The study is only a counting exercise. Momentum resolution, ghost rate etc play important roles, and will be studied. However, the general conclusion would change.

Module



Active gap ~ 200 μm

A naïve calculation

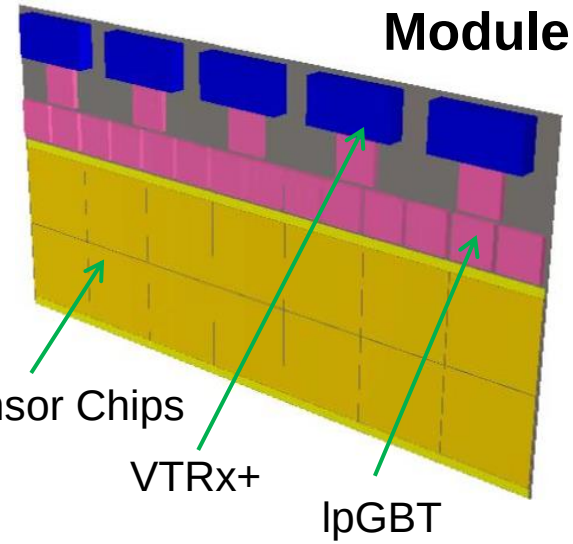
- ~1.4% inefficiency / plane / track
- ~4.2% for 3 hits out of 3 planes
- ~25% for all 6 tracks
- ~21% for all 5 tracks

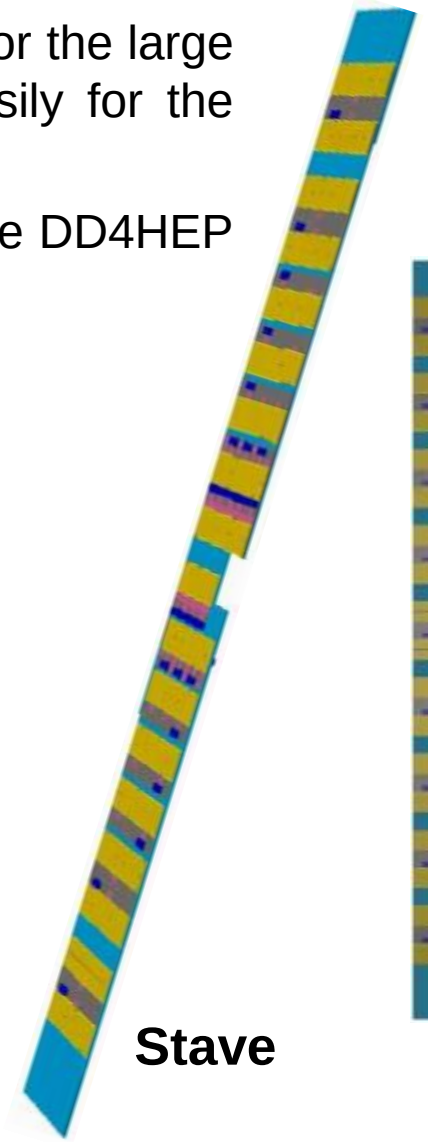
Detector Modelling in The Software

- Detector description has been developed for the large electrode solution. It can be modified easily for the small electrode solution.
- It was initially created based on DDDB. The DD4HEP version now has been well debugged.

Extremely crowded for the inner modules

Module

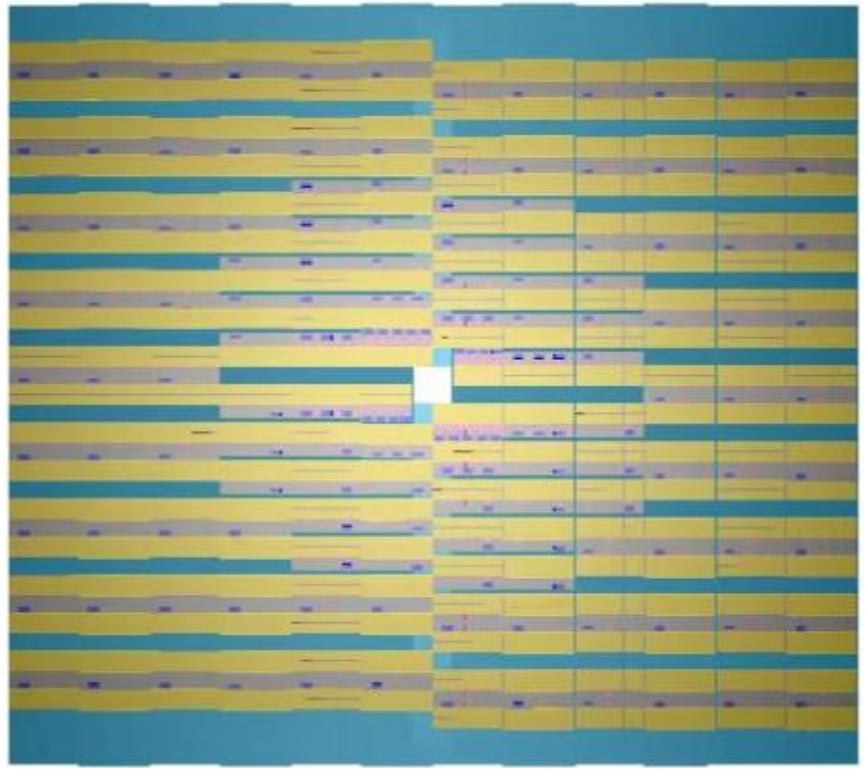




Stave

Plane

(4 planes are identical for now)



Simulation and Reconstruction Software

```
33  #  include "UTDet/DeUTBaseElement.h"
34  #  include "UTDet/DeUTSide.h"
35  #  include "UTDet/DeUTLayer.h"
36  #  include "UTDet/DeUTStave.h"
37  #  include "UTDet/DeUTFace.h"
38  #  include "UTDet/DeUTModule.h"
39  #  include "UTDet/DeUTChip.h"
```

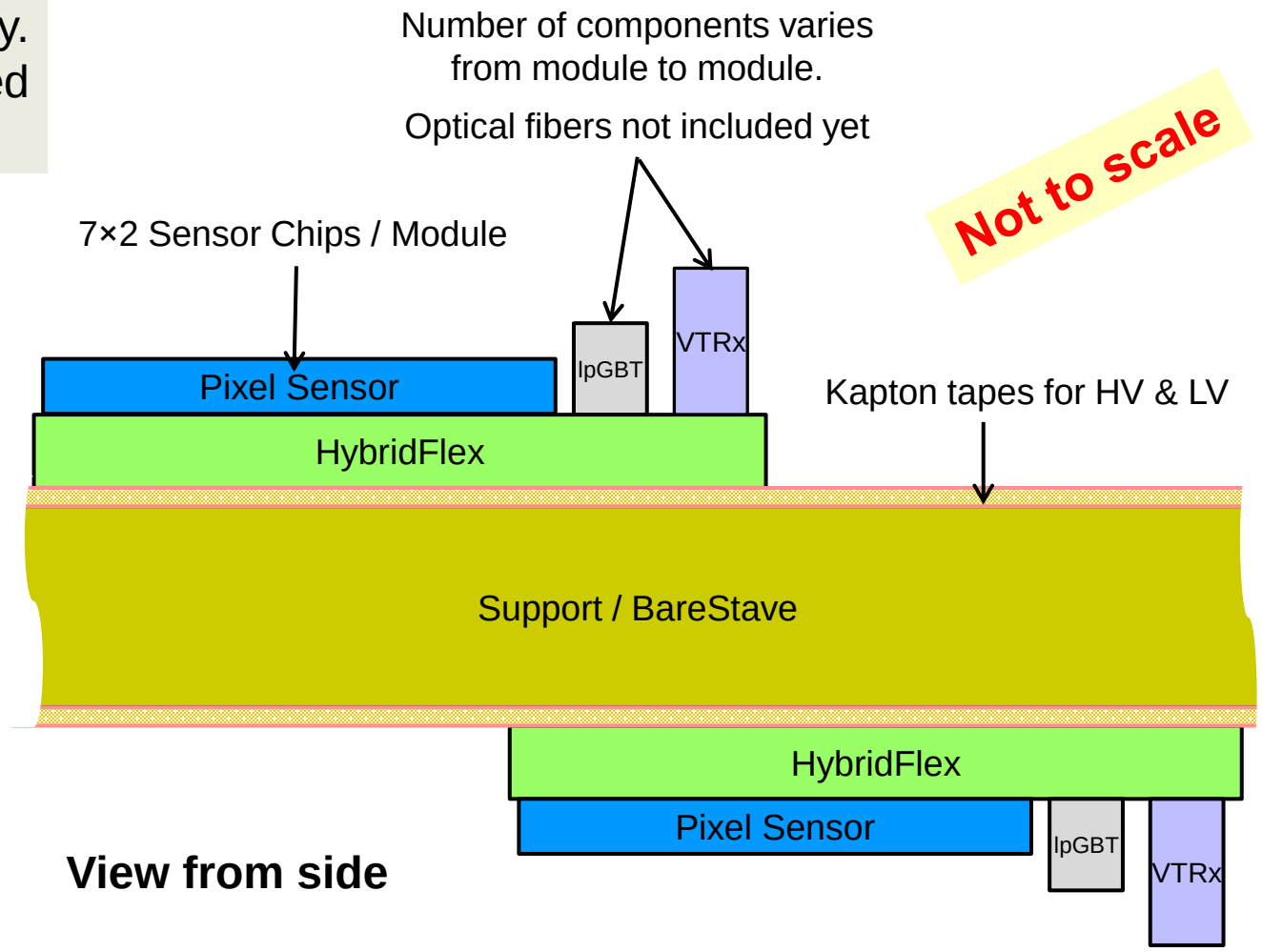
Matching the U2UT geometry

- The DetElement for U2UT, used in the basic implementation of detector description, has been built successfully.
- The focus has been shifted to a full simulation in Gauss (Gaussino) & Boole, and later on reconstruction.
- Detector performance and RawBank format are important for the simulation digitization and design of the encoder/decoder.

Simplified Stave Structure

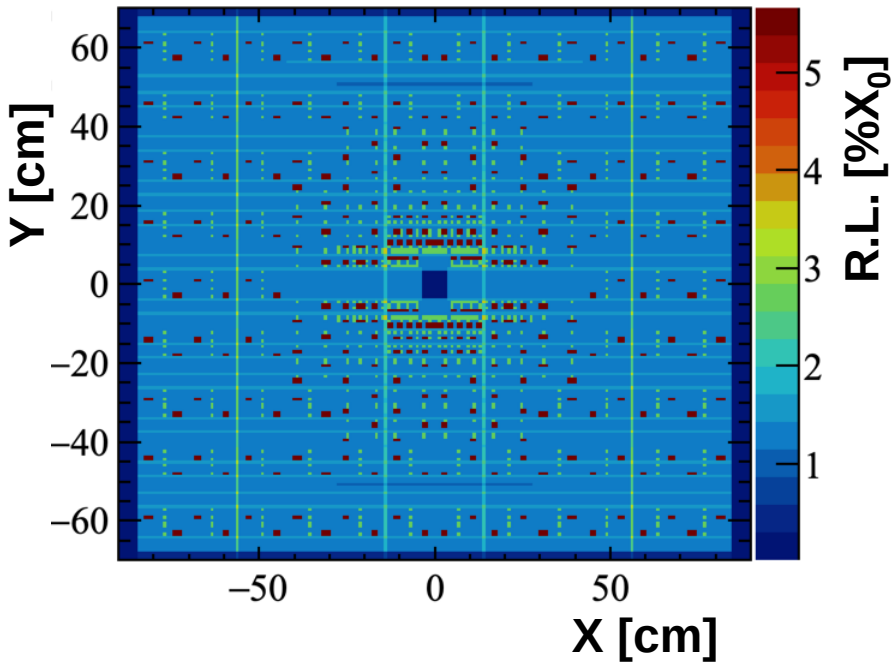
Sizes and materials are preliminary. More precise values will be used when available.

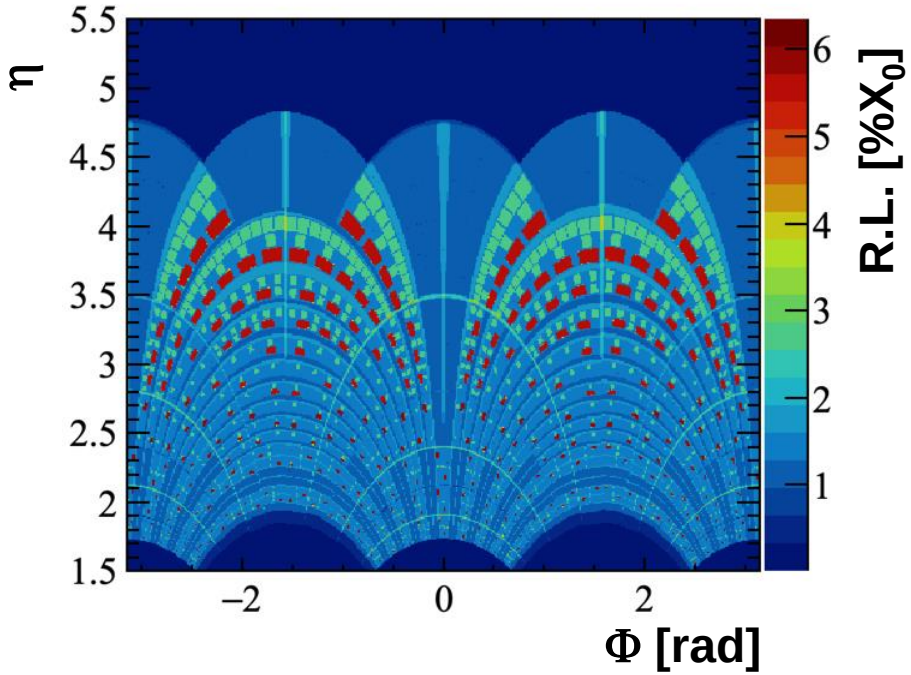
(Unit: mm)	Thickness	W×L
Pixel Sensor	0.200	20.2 × 21.4
lpGBT	1.250	9 × 9
VTRx+	4.000	10 × 20
HybridFlex	0.300	142 × 75
Kapton Tape	0.100	142 × full
BareStave	4.000	142 × full



View from side

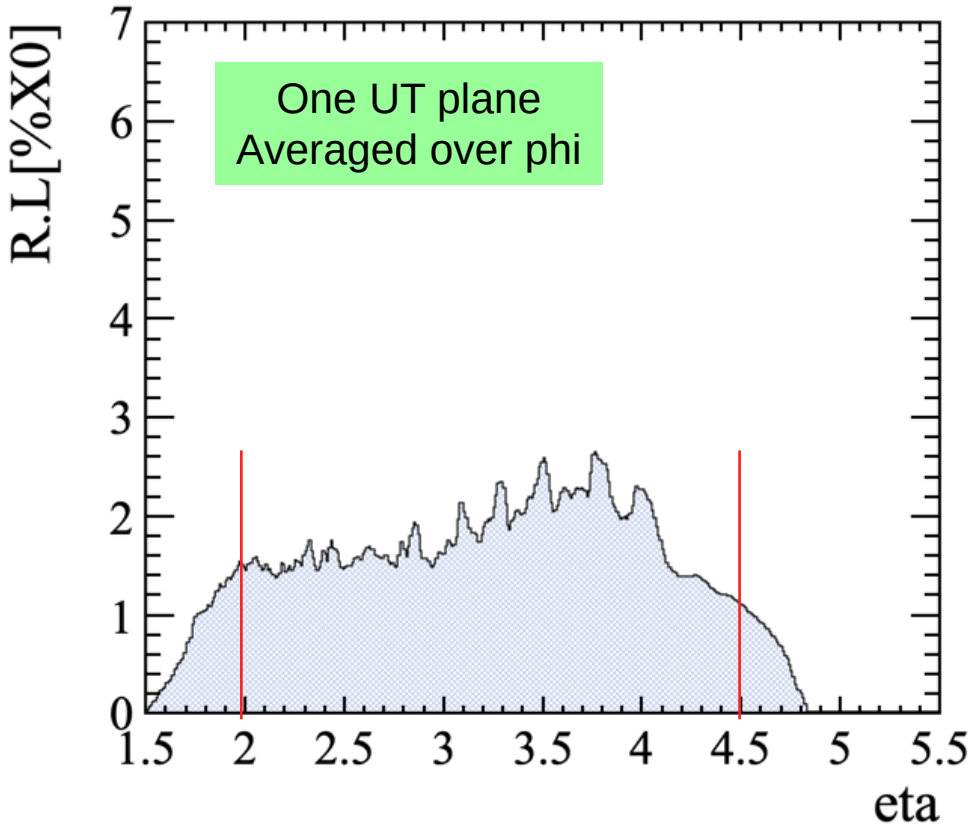
Radiation Length of A U2UT Plane





- We don't have detailed composite of VTRx+ and lpGBT.
- Some other electronic components are not included yet.

Break-down Radiation Length



(Preliminary)	Thickness [mm]	RL (2<η<4.5) [% X_0]
Pixel Sensor	0.200	0.24
lpGBT	1.250	0.25
VTRx+	4.000	0.27
HybridFlex	0.300	0.42
Kapton Tape	0.100	0.14
BareStave	4.000	0.21
One plane	**-**	**1.54**

Need better info

Need a thinner design

- This is a first step to get a rough idea on material budget.
- More precise information and better designs will be included.

Sensor Specification

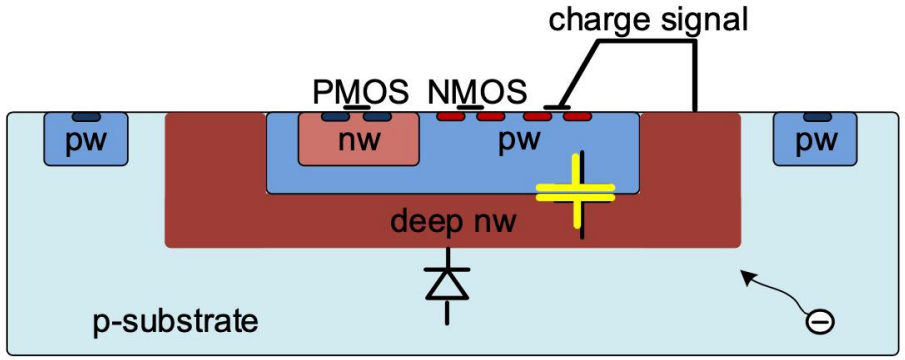
Characteristics	LV-CMOS	HV-CMOS
Chip size	3.5 × 3.5 cm^2	2.0 × 2.0 cm^2
Pixel size	30 × 30 μm^2	50 × 150 μm^2
Chip thickness	~ 100 μm	
Position resolution	5-10 μm	15, 40 μm
Time resolution	O (1) ns	
Power consumption	100 – 300 mW/cm^2	
Radiation dose	3×10^{15} n_{eq}/cm^2, or 240 Mrad TID	
Data rate per chip	Up to 30 Gb/s	Up to 9 Gb/s

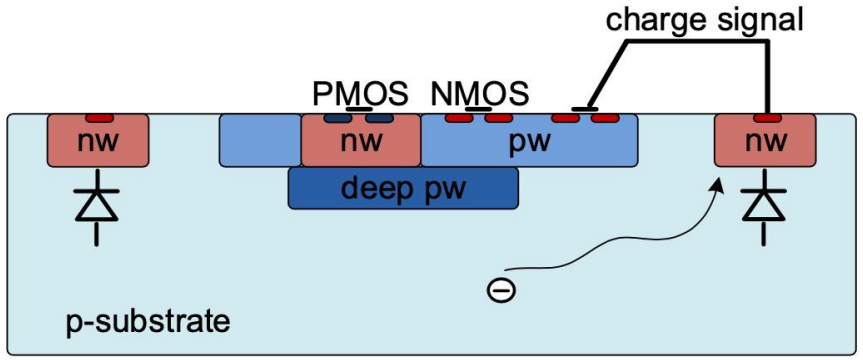
- Depends strongly on the desired time resolution.
- Time resolution O(1) ns is for BXID tagging.

⇒ the cooling requirements

- The radiation hardness requirement is tougher than the MT.
- HV-CMOS may be more radiation hard than LV-CMOS.
- It may be possible to replace the inner-most modules beyond certain radiation dose.

MAPS Technologies For UT





Large collection electrode

- Circuitry inside the charge collection well
- Large uniform electric field
- On average shorter drift path
- Better radiation hardness (less trapping)
- Very large sensor capacitance (both pw and dnw)

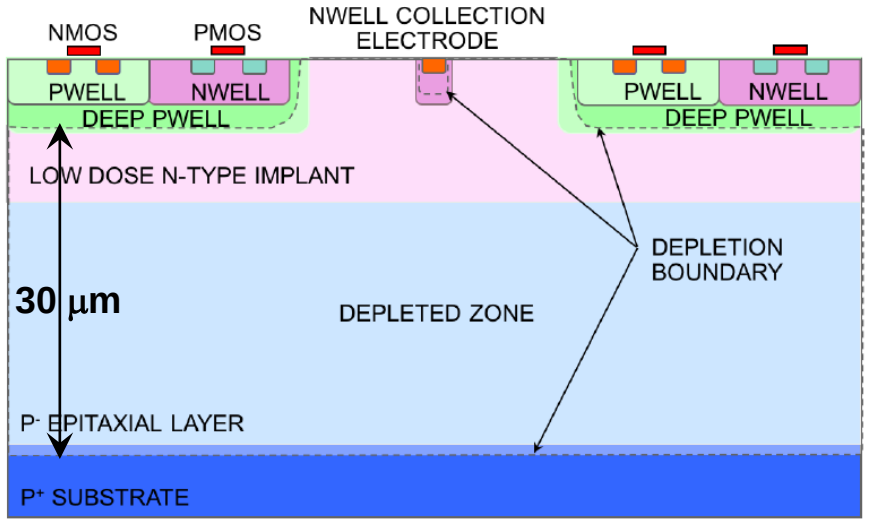
Small collection electrode

- Circuitry outside the charge collection well
- Optimization of little low-field regions
- On average longer drift path
- Radiation hardness needs process modifications
- Very small sensor capacitance

- UT has special needs: radiation hardness 3×10^{15} n_{eq}/cm^2, and 240 Mrad TID; time resolution O(1) ns for BXID tagging with low power consumption 100-300 mW/cm^2.
- Both solutions have pros and cons. We want to take some time and choose a better technology.
- Research activities on small electrode (e.g. MALTA2), and large electrode (e.g. AtlasPix3, MightyPix, …). Hope to converge by 2025.

TowerJazz MALTA2 Chip

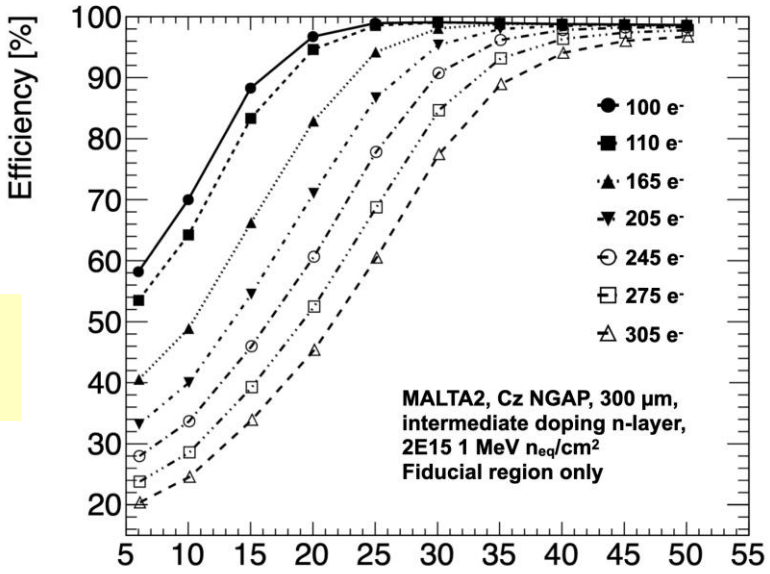
180 nm TowerJazz CMOS imaging technology
designing team: CERN, Bonn University, CPPM



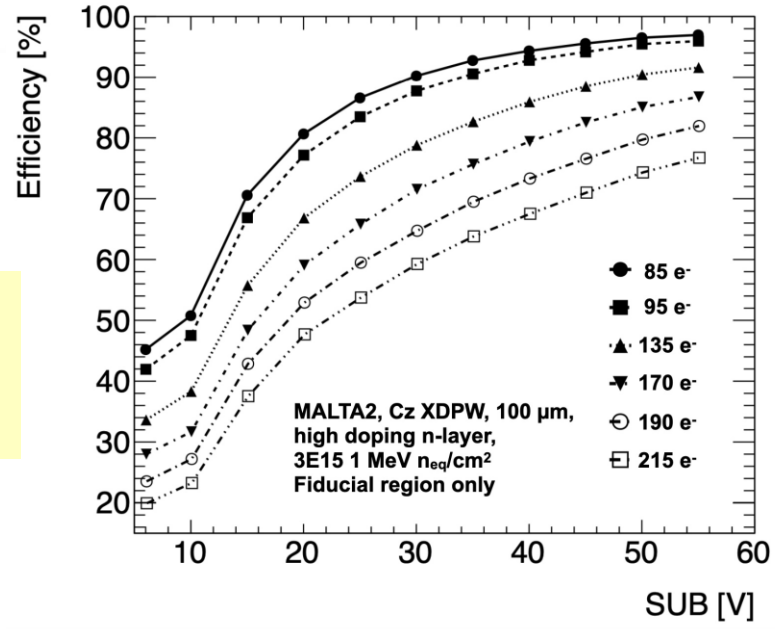
TowerJazz modified process :

- low dose n-type implant ensures uniform depletion of high resistivity epitaxial layer
- active region : 25 - 30 µm
- available total thickness : 50 - 100 - 300 µm
- Bias voltages: 6 - 20 V (substrate), 6V (pwell)

2×10^{15} n_{eq}/cm^2
300 µm thick



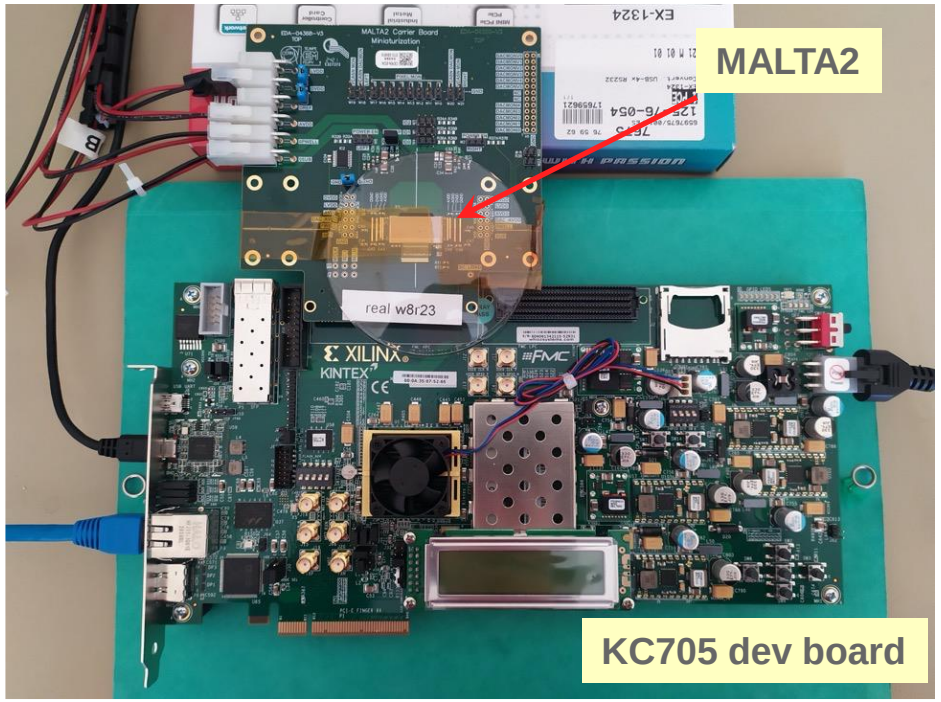
3×10^{15} n_{eq}/cm^2
100 µm thick
@ -20°C



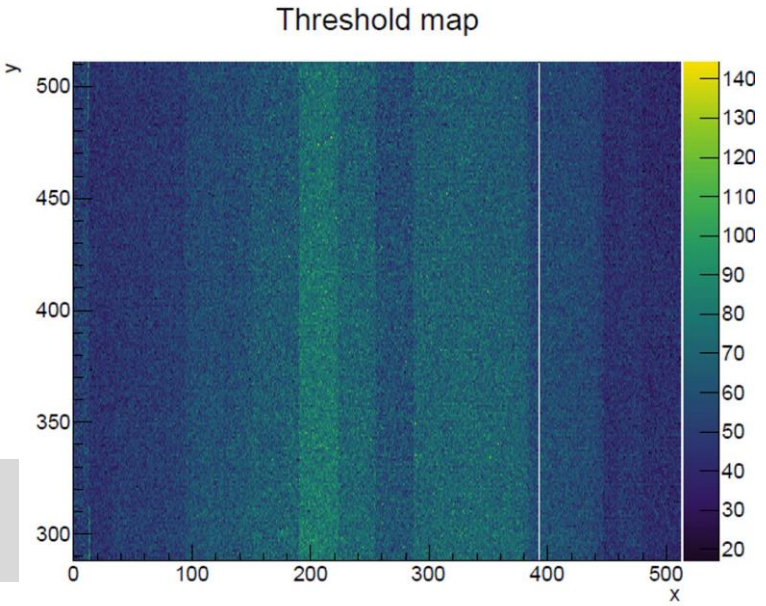
Extracted from Pixel 2022 https://indico.cern.ch/event/829863/contributions/4479493

MALTA2 Test @ CEA-IRFU

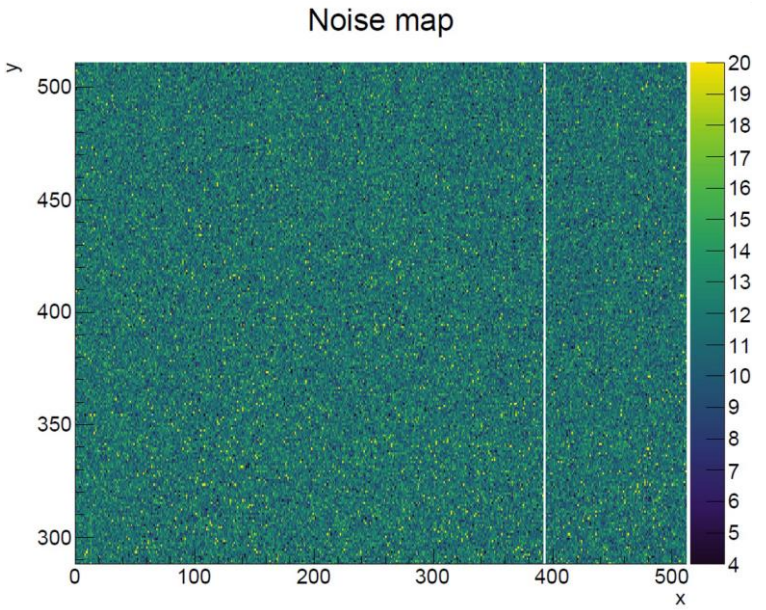
- MALTA2 is tested at CEA-IRFU. Kintex-7 dev board is used to control and readout.
- Threshold and noise were measured in room temperature.
- Common threshold set to ~60 e ⇒ dispersion ~13.7 e.
- Average noise ~12 e within expectation, homogenous over the whole matrix.



Threshold ~ 60 e
dispersion ~ 13.7 e

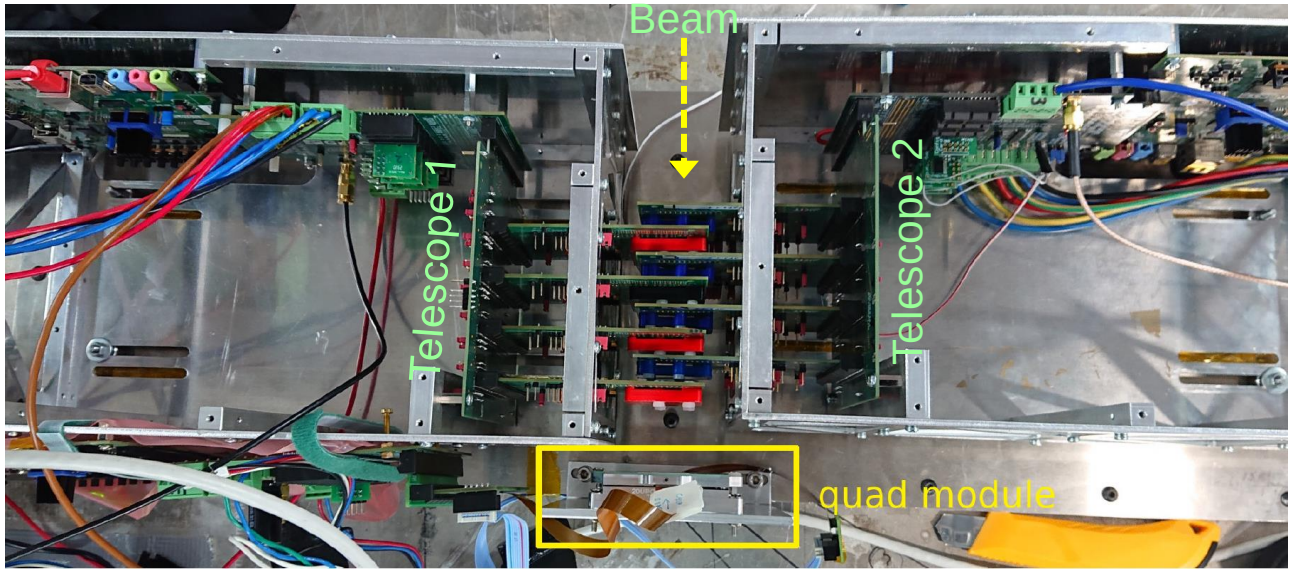


Noise ~ 12 e

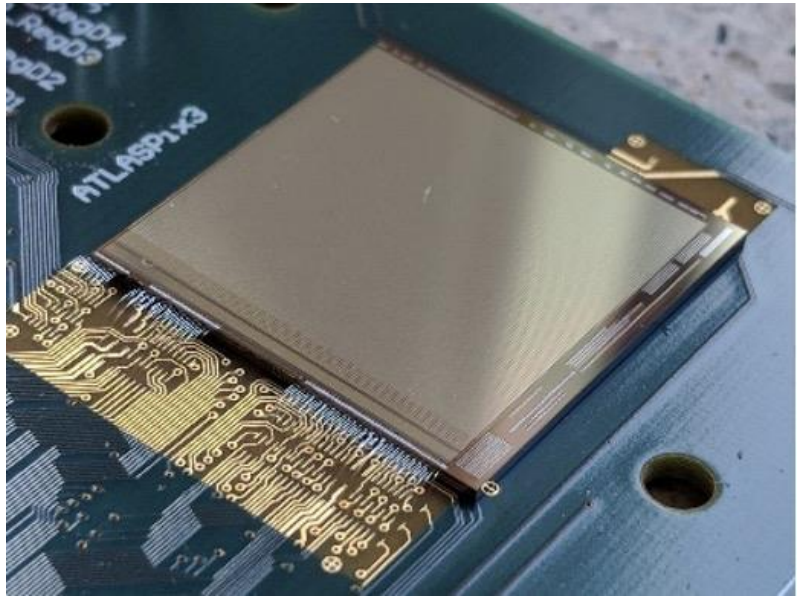


AMS/TSI ATLASPix Chip

- ATLASPix3 chip of large electrode (aka HV-CMOS)
  - TSI 180nm HV process on 200 Ωcm substrate
  - Time resolution for every pixel: 6.7± 0.5 ns without correction and 4.1±0.1 ns with ToT correction.
  - Power consumption ~160 mW/cm^2.
- Testbeam at DESY in April 2022 using electron beam up to 6 GeV, in form of 2 telescopes and 1 quad module.



ATLASPix3 chip



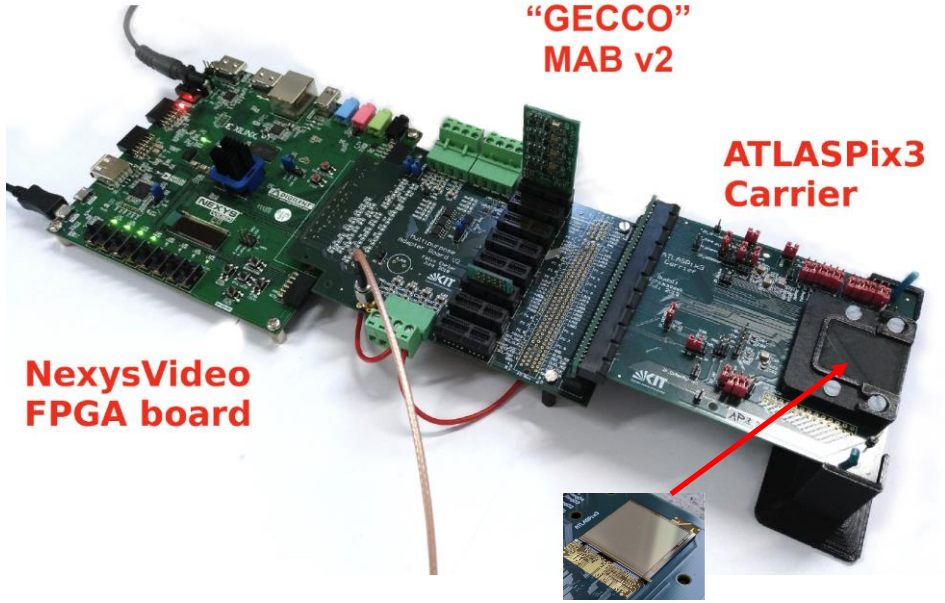
I. Peric et al., High-Voltage CMOS Active Pixel Sensor, IEEE JSSC, Volume: 56, Issue: 8, Aug. 2021 https://ieeexplore.ieee.org/document/9373986

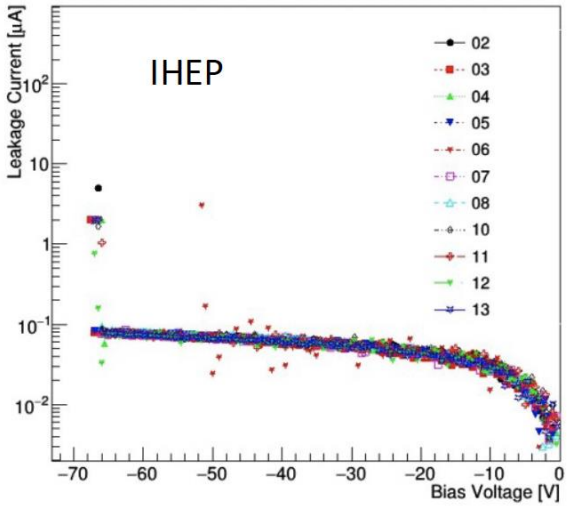
https://indico.ihep.ac.cn/event/17020/contributions/118948/attachments/64226/74990/MightyPix_IvanPeric_forcepc_nt.pptx

https://indico.cern.ch/event/1215937/contributions/5262920/attachments/2592075/4473451/20230213_cepcSiTracker_LIYiming.pdf

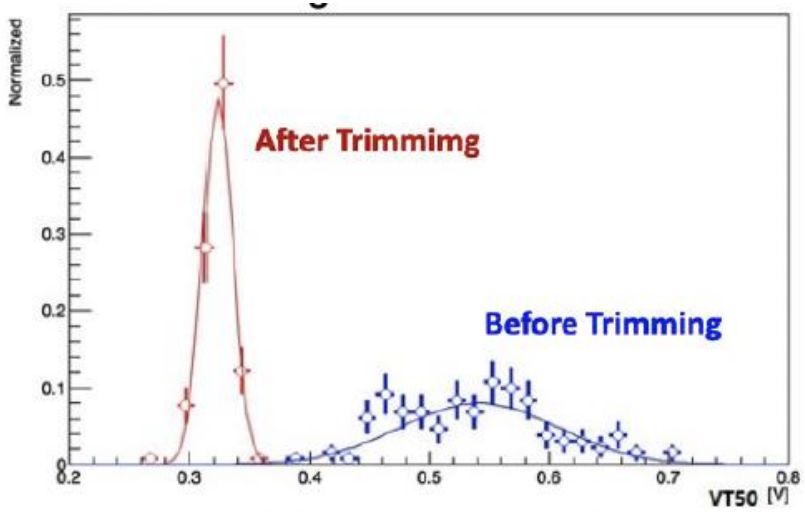
ATLASPix3 Test @ IHEP

- The ATLASPix3.1 chips had been tested at IHEP, readout using a GECCO system.
- Threshold trimming and noise performance, noise ~60 e for threshold ~1700 e.
- Tested in cosmic ray and various radioactive sources.

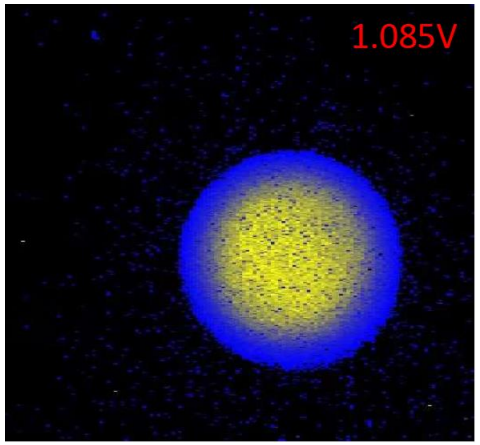




IV measurement



Threshold trimming

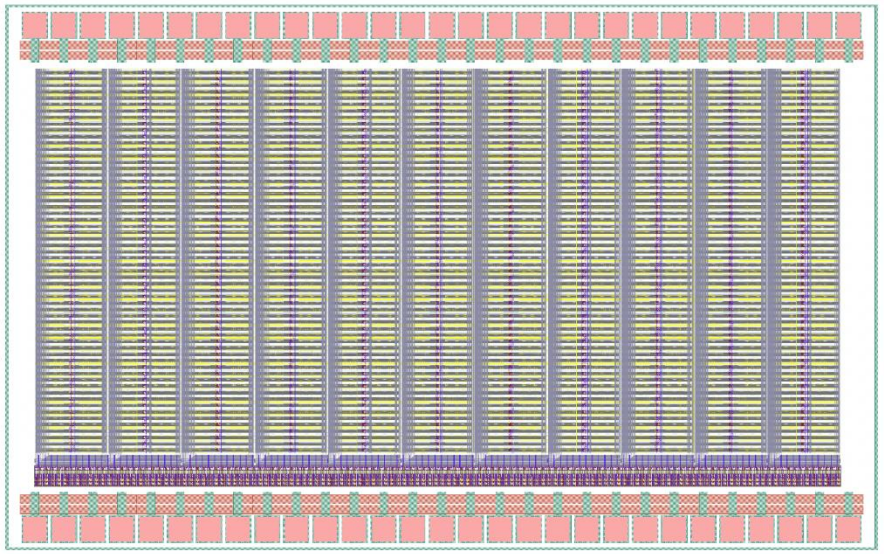


Hitmap with Fe55 source

Attempts for Alternative Foundries

HLMC 55 nm HV process

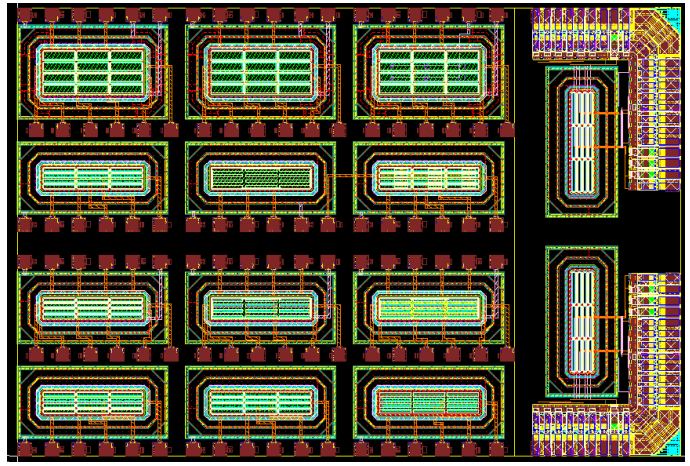
- Pixel array being designed by KIT and IHEP, pixel size 25×150 μm^2
- Caveat: wafer with high-resistance substrate not yet supported.
- Still seeking MPW opportunity



Preliminary design of pixel array using HLMC 55 nm by KIT

SMIC 55 nm process

- HV and normal (Low-Leakage) process available
- Possible to use high-resistance wafer
- A MPW submission in Oct 2022 with LL process. The design contains a few passive sensor diodes and amplifiers
- Seeking MPW opportunity in 2023 with HV process



Schematics of sensor diode design using SMIC 55 nm by IHEP / HNU

Summary

- The Upgrade 2 UT R&D starts to gain momentum, aiming for a TDR in ~2026.
  1) Currently we consider the detector coverage in FTDR reasonable; Descoping from 4 planes to 3 is not preferred.
  2) Detector modelling and description are done in DDDB & DD4HEP. Basic detector element code is ready, allowing study of the material budget. Focus has been shifted to Gauss/Boole simulation and Moore reconstruction.
  3) We are studying MALTA & ATLASPix chips, the examples of small and large electrode CMOS chips from TowerJazz and TSI, respectively. We are also attempting for alternative foundries with smaller feature size.
- The UT project finished installation successfully, and entered the commissioning stage. Hopefully more hands are freed out for the upgrade II R&D.
- We welcome more institutes and people to join the upgrade II activities.

Thanks to my colleagues for providing materials, especially Fabrice Guilloux, Stefano Panebianco, Yiming Li, Xuhao Yuan, Xiaokang Zhou, Ruoshi Dong, Zhiyu Xiang, Shuqi Sheng, Mingjie Feng, …