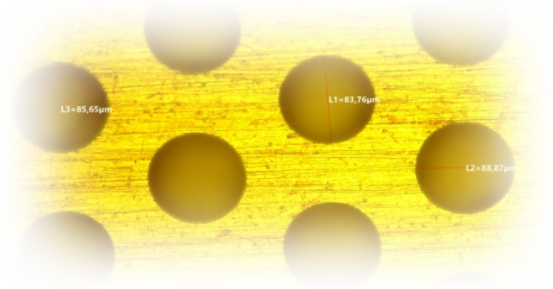
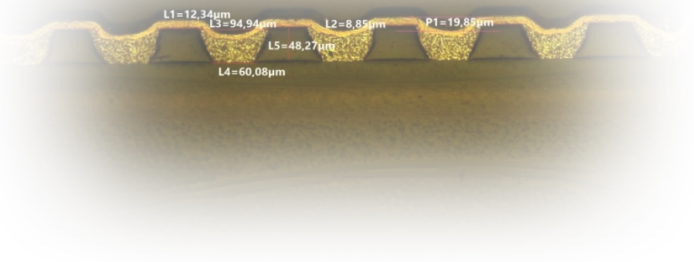
6th workshop on LHCb upgrade II
Barcellona 29-31 March

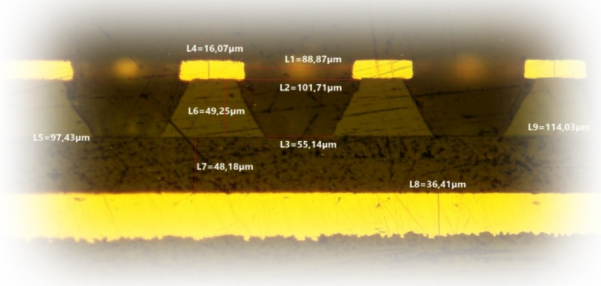
The micro-RWELL for R1/R2

Status & plans

E. Santovetti
for the micro-RWELL LHCb group
LNF, Roma2, Bari







Outline

- Detector choice
  - experiment requirements
  - Micro-RWELL features
- FE electronic
- Summary and outlooks

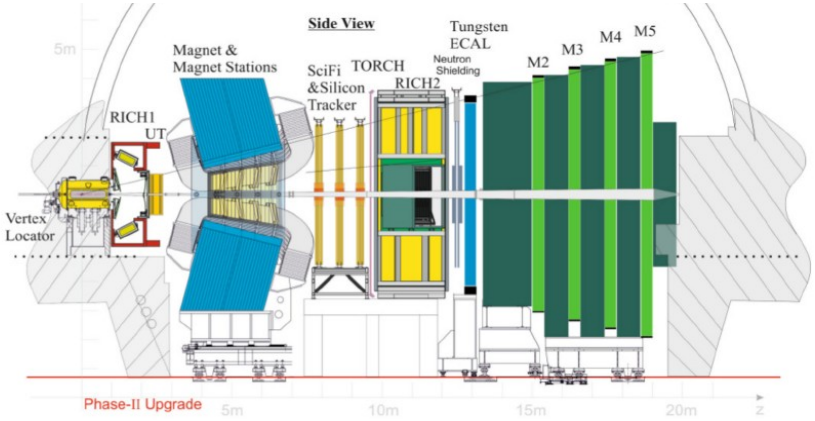
LHCb upgrade II (Run5 – Run6)

LHCb muon apparatus Run5 – Run6 option detector requirements

- Rate up to **1 MHz/cm²** on detector single gap
- Rate up to **700 kHz** per electronic channel
- Efficiency quadrigap >=99% within a BX (25 ns)
- Stability up to **1C/cm²** accumulated charge in 10y at M2R1, G=4000

Detector size & quantity (4 gaps/chamber - redundancy)

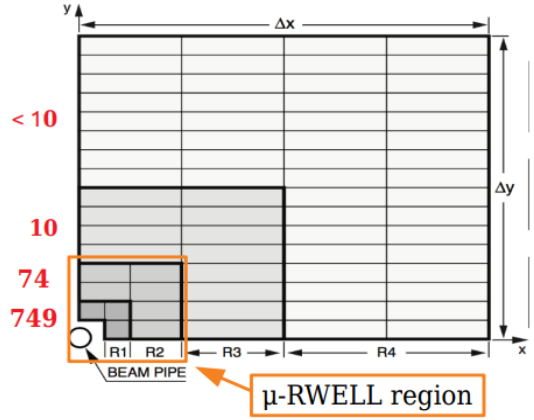
- **R1÷R2: 576 detectors, size 30x25 to 74x31 cm², 90 m² detector (130 m² DLC)**
- ~~R3: 768 detectors, siz 120x25 to 149x31 cm², 290m² det.~~
- ~~R4 : 3072 detectors, size 120x25 to 149x31 cm², 1164 m² det~~.



Rates (kHz/cm^2)	M2	M3	M4	M5
R1	749	431	158	134
R2	74	54	23	15
R3	10	6	4	3
R4	8	2	2	2

Area (m^2)	M2	M3	M4	M5
R1	0.9	1.0	1.2	1.4
R2	3.6	4.2	4.9	5.5
R3	14.4	16.8	19.3	22.2
R4	57.6	67.4	77.4	88.7

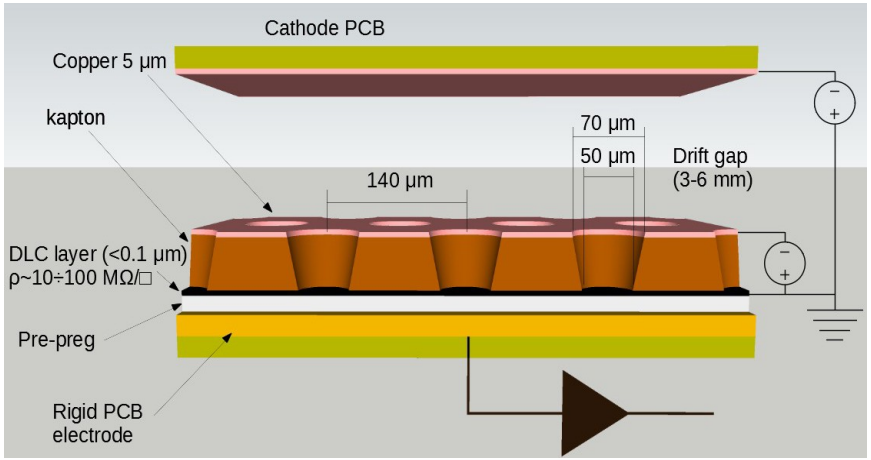
M2 station - max rate (kHz/cm²)



The μ-RWELL

PoS(MPGD2017)019

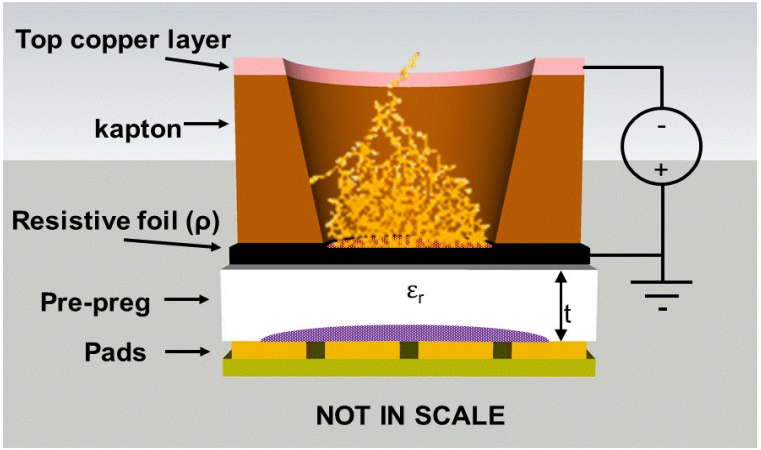
G. Bencivenni et al., The micro-Resistive WELL detector: a compact spark-protected single amplification-stage MPGD, 2015 JINST 10 P02008



The **μ-RWELL** is a **resistive MPGD** composed of two elements:

- **Cathode**
- **μ-RWELL_PCB:**
  - a **WELL** patterned **kapton foil** (w/**Cu-layer on top**) acting as **amplification stage**
  - a **resisitive DLC** layer(*) w/ **ρ ≡ 10÷100 MΩ/cm**
  - a standard **readout PCB** with **pad/strip** segmentation

(*) DLC foils are currently provided by the Japan Company – BeSputter

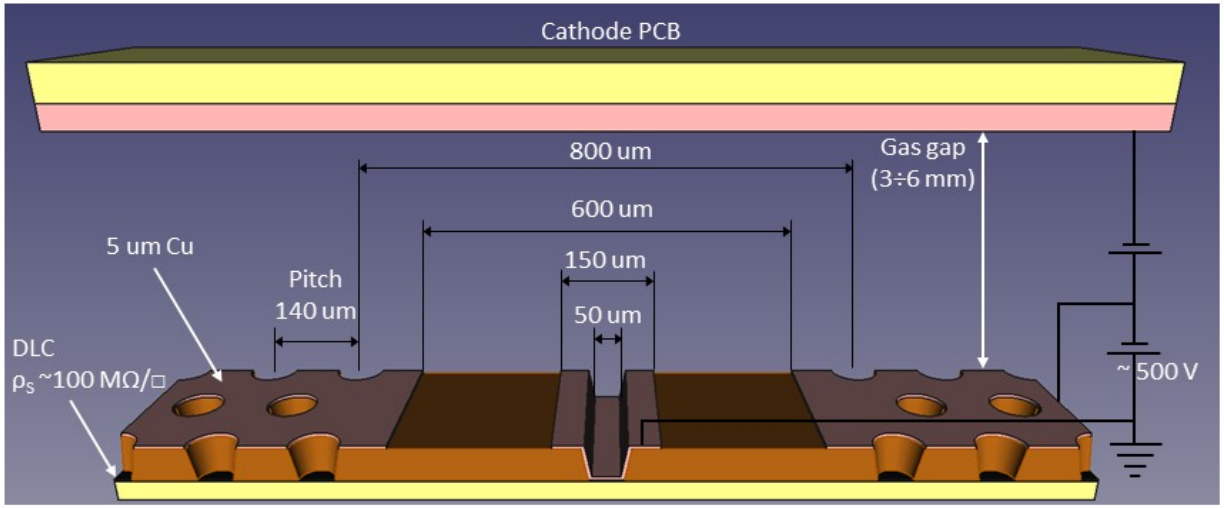


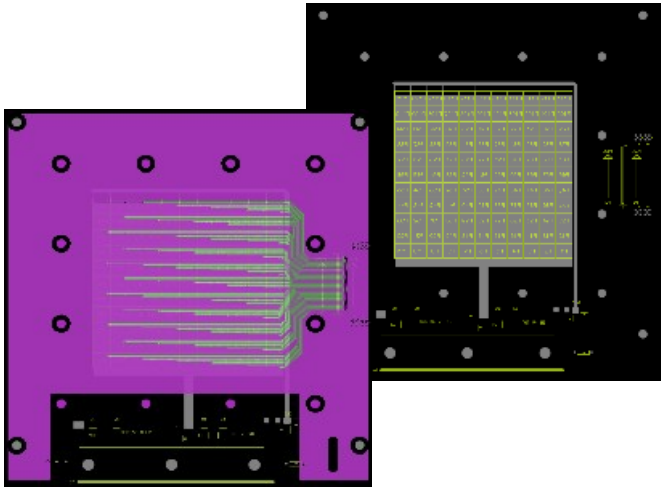
The **"WELL"** acts as a **multiplication channel** for the ionization produced in the drift gas gap.

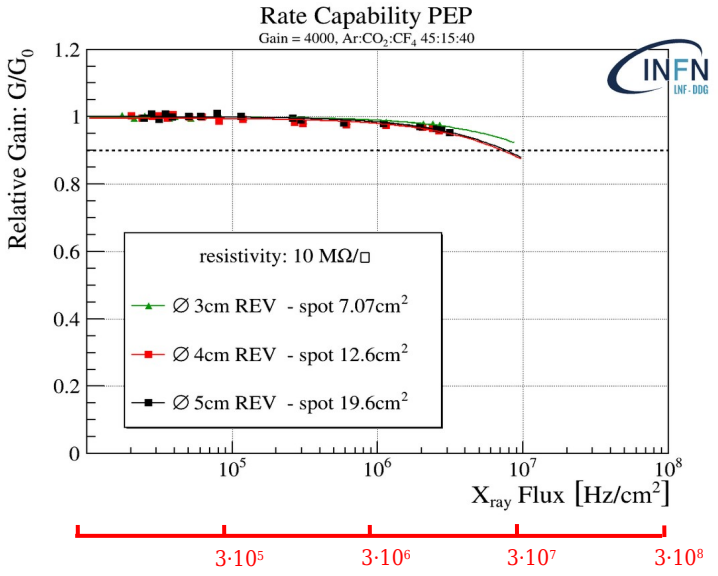
The **resistive stage** ensures the **spark amplitude quenching.**

Drawback: capability to operate at high particle fluxes reduced, but **largely recovered** with appropriate **grounding schemes** of the **resistive layer**

The HR layout







The **PEP** layout (Patterning – Etching – Plating) is the **state of art** of the **high rate** layout of the μ-RWELL developed **for LHCb**

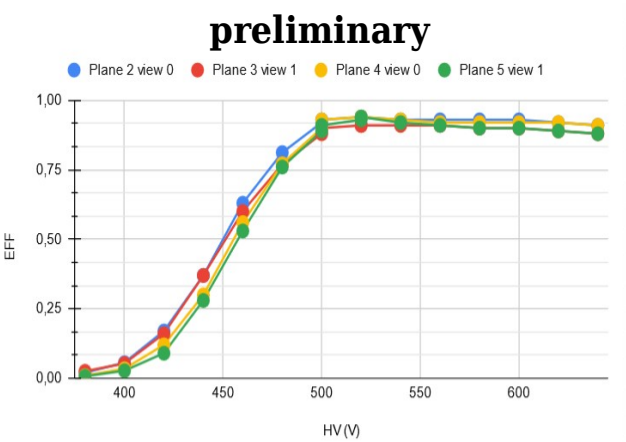
- **Single DLC** layer
- **Grounding line from top** by kapton etching and plating (pitch down to 1 cm)
- **No alignment** problems
- **High rate** capability
- **Scalable to large size** (up to 1.2x0.5 m for the upgrade of CLAS12)

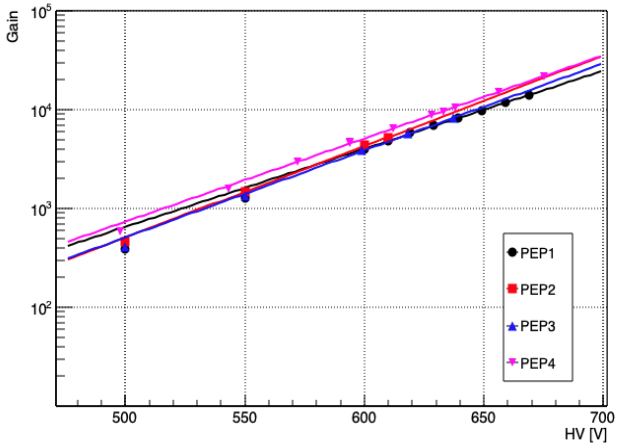
QA & QC

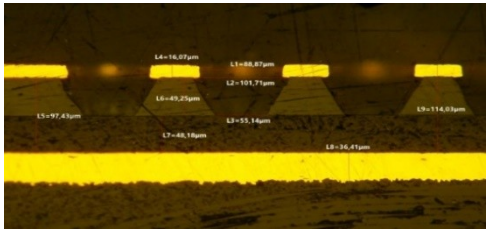
The technology has been **largely improved** in the last year, thanks to the introduction of the "**dry-electrical-cleaning",** a sort of a hot HV conditioning allowing a soft cleaning of the residual imperfections of the detector manufacturing.

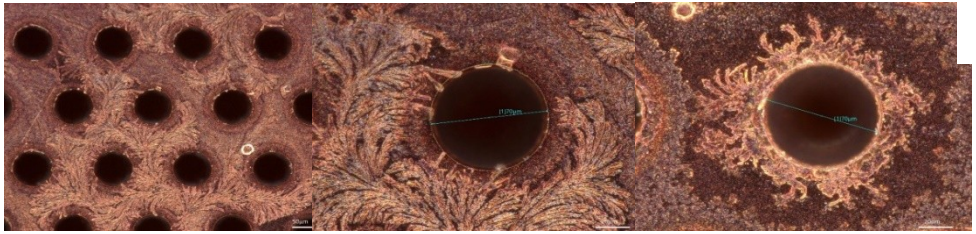
Detector stability improved: up to **150V** large plateau, **estimated gain up to 2×10^4** (to be measured).

Optical metallographic survey (in ELTOS) as well as **SEM analysis** (at CERN) are used to take all construction steps under control as well as checking effects for possible aging/etching (by fluorine …).









μ-RWELL – single gap efficiency

Detector | **FEE**

single gap EFFICIENCY = Rate Capability × Active Area × FEE THR × σ_t: eff in 25ns = **0.887÷0.897**

Rate Capability	Active Area	FEE THR	σ_t: eff in 25ns
1.00	**0.955÷0.964**	**0.965**	**0.963**

w/ Ar:CO_2:CF_4 45:15:40
σ_t = 6ns (conservative)

10% gain drop @ 1MHz/cm² → no efficiency drop

Dead zone <5% (layout dependent)

Gas Gain = 4000
w/ **Ar:CO_2:CF_4 45:15:40**
μ (10GeV, 35.8 e^-I^+ in 3mm)
FEE THR = 5fC

	pad X [cm]	pad Y [cm]	pad Area [cm²]	max rate [kHz/cm²]	max x pad [kHz/pad]	correlated fraction
M2R1	0.90	0.89	0.80	620	**494**	0.26
M2R2	0.89	1.80	1.61	280	**450**	0.31
M3R1	0.96	0.97	0.93	290	**270**	0.17
M3R2	0.96	1.94	1.87	80	**150**	0.26
M4R1	1.04	1.03	1.07	210	**224**	0.35
M4R2	1.04	2.09	2.16	45	**97**	0.39
M5R1	1.11	1.11	1.23	250	**308**	0.31
M5R2	1.11	2.20	2.44	50	**122**	0.39

μ-RWELL – 4 stations efficiency

single gap EFFICIENCY = **0.887÷0.897** → **4 gaps for each station** → **4 stations**

Option (1) – 4 gaps **OR** (e.g. **R1**)

Station efficiency, taking into account correlated hit and FEE dead time (100 ns)

M2R1 – 0.987
M3R1 – 0.995
M4R1 – 0.992
M5R1 – 0.990

M2⊕M3⊕M4⊕M5 = 0.965

Option (2) – **Majority** 2 of 4 (e.g. **R1**)

Station efficiency, taking into account correlated hit and FEE dead time (100 ns)

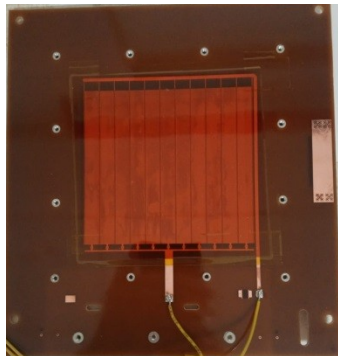
M2R1 – 0.976
M3R1 – 0.987
M4R1 – 0.985
M5R1 – 0.983

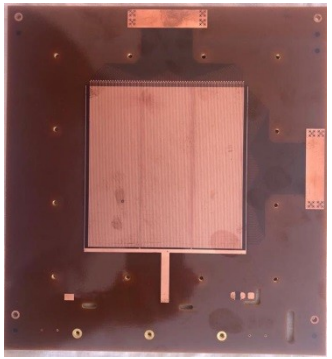
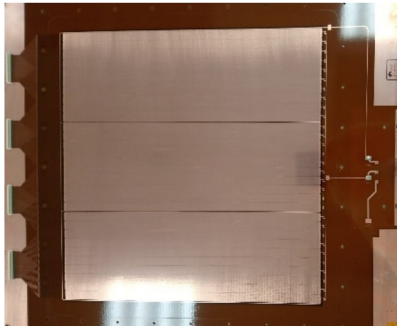
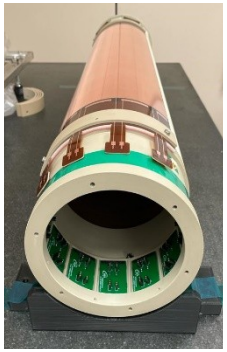
M2⊕M3⊕M4⊕M5 = 0.933

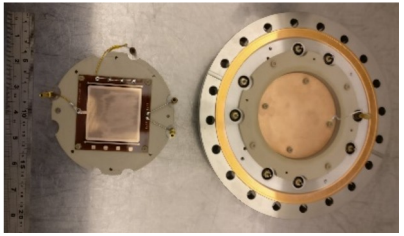
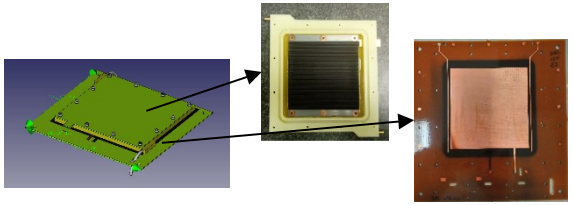
Summary – R1/R2 and gas mixtures

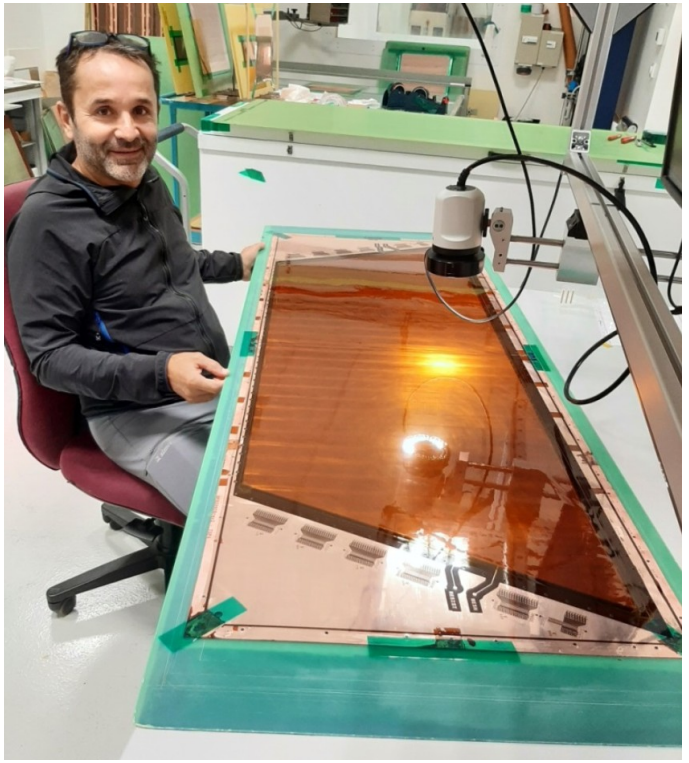
	$Ar:CO_2:CF_4$ 45:15:40 σ_t = 6ns THR=5fC		**$Ar:CO_2$:iso 68:30:02** σ_t = 8ns THR=5fC	
	4 stations		4 stations	
	OR	**MAJ**	**OR**	**MAJ**
R1	0.965	0.933	0.940	0.665
R2	0.973	0.947	0.951	0.684

Technology spread



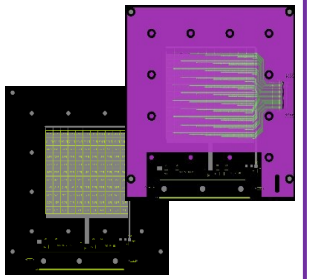


The **improvement of the quality and yield** is a clear **by-product of the technology spread** (in particular CLAS12 upgrade at JLAB).

Technology transfer and production cycle

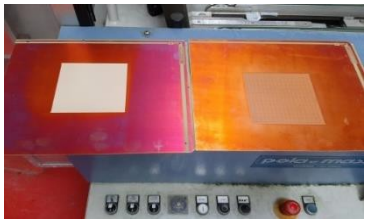
AIDA innova
EU-project

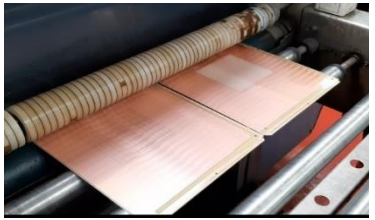
LAYOUT design

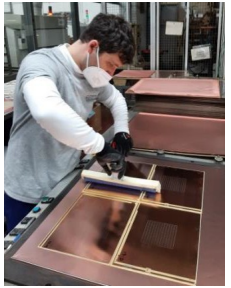


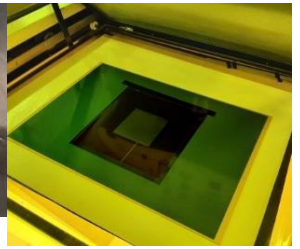
DLC foil production (*)

PCB production

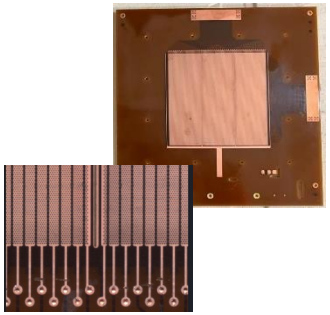








Final detector manufacturing



***DLC Magnetron Sputtering machine co-funded by INFN- CSN1**

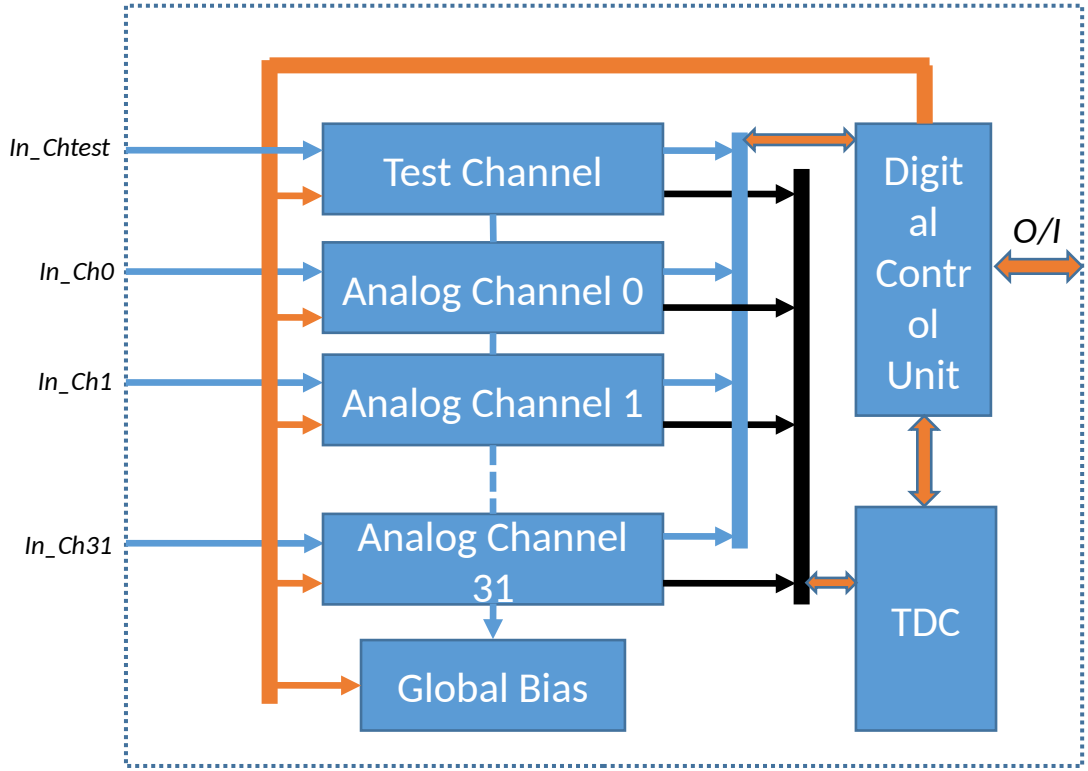
FE Electronics

- FE electronics has a **crucial role** in the detector efficiency: dead time, S/N ratio and threshold …
- The number of channels is very large (~ 150k) on quite small detector sizes → engineering very important.
- We have selected a chip (**FATIC** - Bari INFN) which seems to be right for us even if something will have to be changed to adapt it to our needs

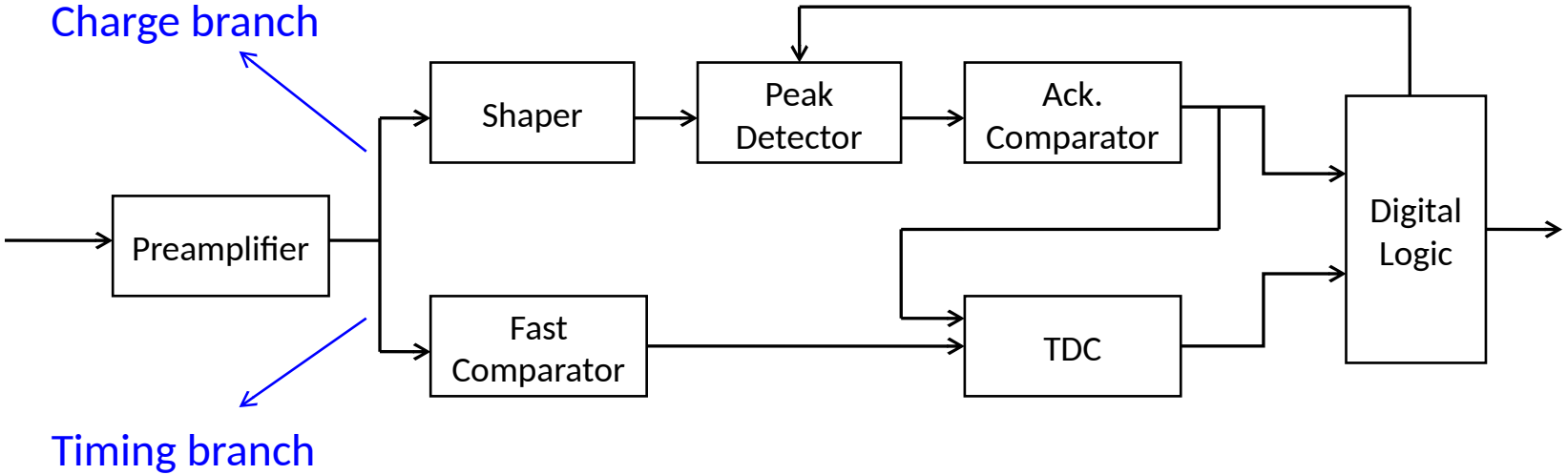
FATIC architecture

Features:

- Technology: TSMC 130 nm
- 32 channels
  - **Programmable** polarity, gain and peaking time
  - **Charge** and **time** measurement
  - TDC resolution: 100 ps
- Calibration, Bias and Monitoring
  - **Charge injection** calibration
  - Programmable biases (currents and voltages)
  - Monitoring ADC (12 bit SAR)
- 320 Mbps serial link, **lpGBT** compatible
- Power supply 1.2 V
- Radiation hardness: up to 100 Mrad



Channel block diagram



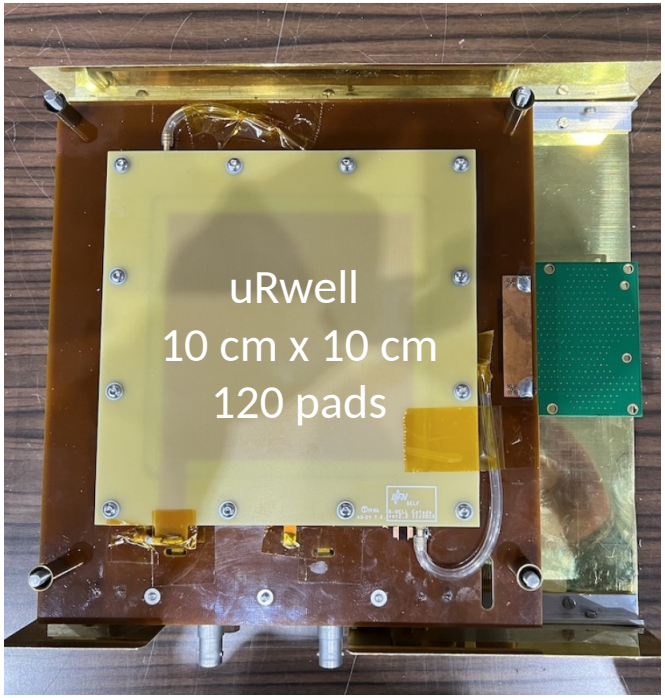
Preamplifier features:
- CSA operation mode
- Input signal polarity: positive and negative
- Recovery time: adjustable

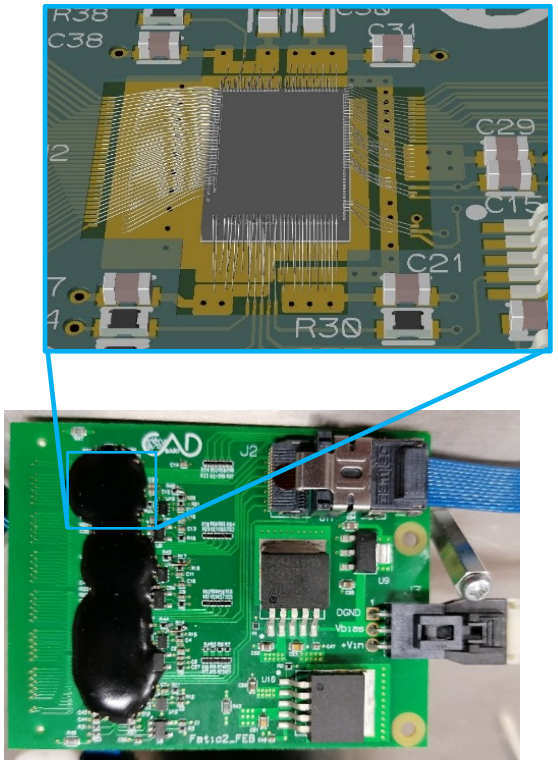
CSA mode:
- Programmable Gain: 10 mV/fC ÷ 50 mV/fC
- Peaking time: 25 ns, 50 ns, 75 ns, 100 ns

Timing branch:
- Measures the arrival time of the input signal
- Time jitter: 400 ps @ 1 fC & 15 pF (Fast Timing MPGD)

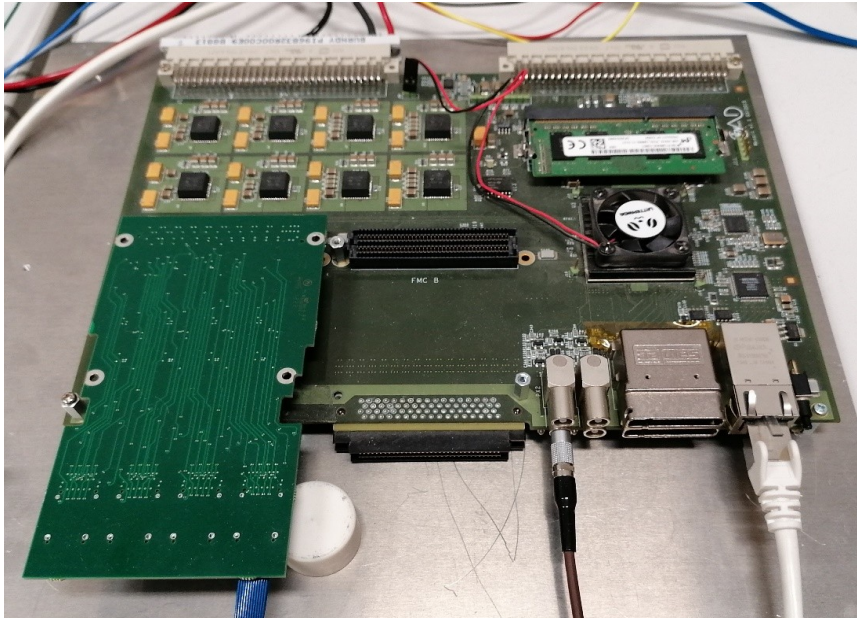
Charge branch:
- Acknowledgment of the input signal
- Charge measurement: dynamic range > 50 fC, programmable charge resolution

Test setup





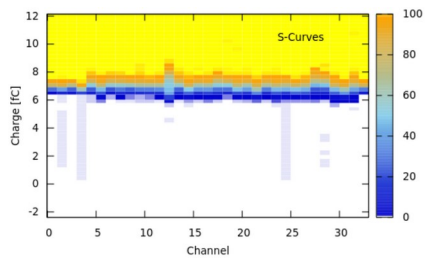
Front End Board
- 4 x FATIC2
- 128 channels

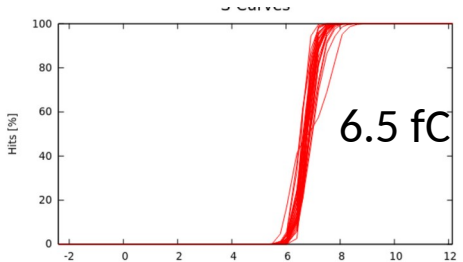


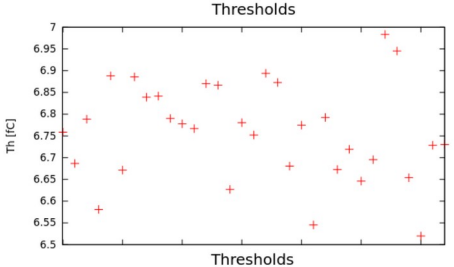
MOSAIC DAQ board + FMC adapter
- Up to 4 FEB

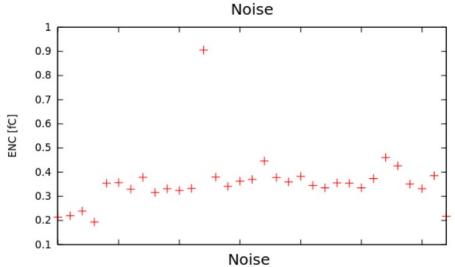
Hardware ready to read up to 4 Front-End boards (4 x 128 channels)

Measure: charge discriminator

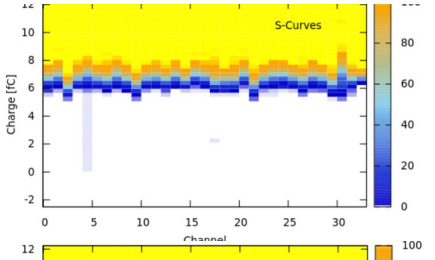


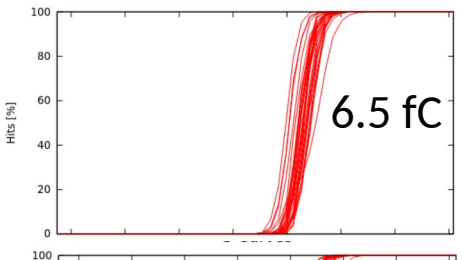


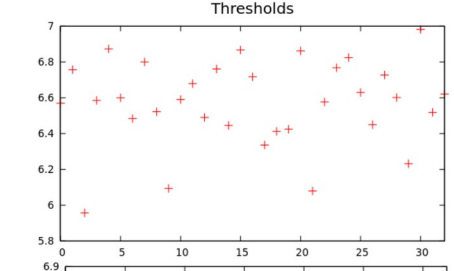


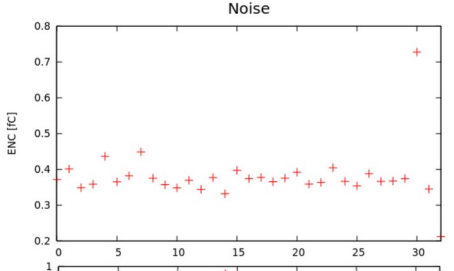


Chip-0

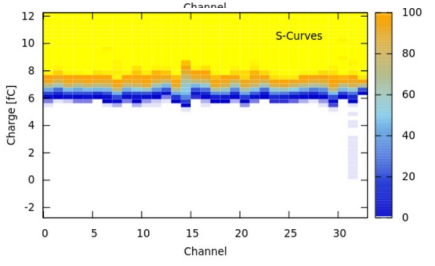


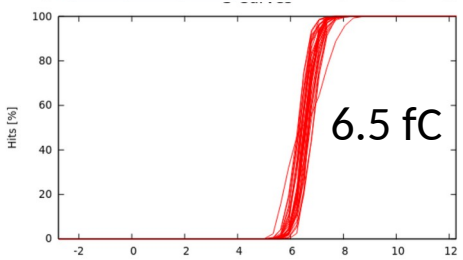


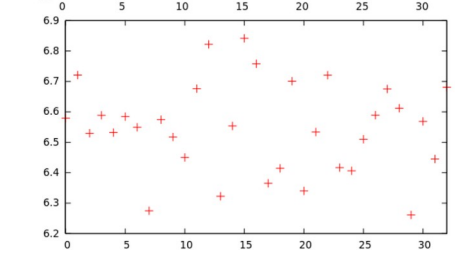


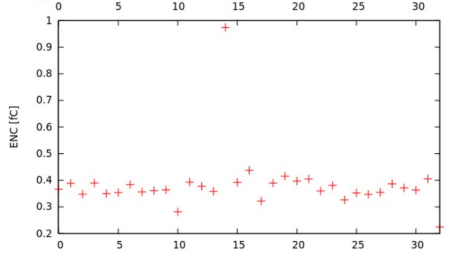


Chip-1

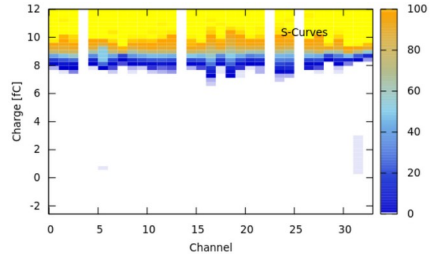


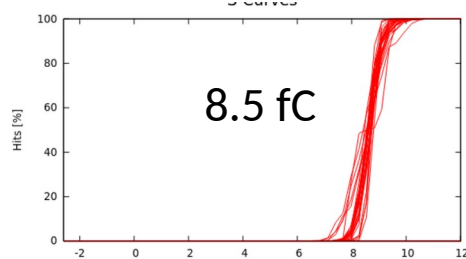


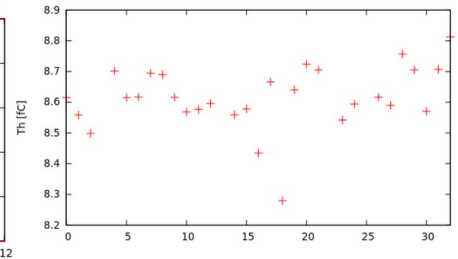


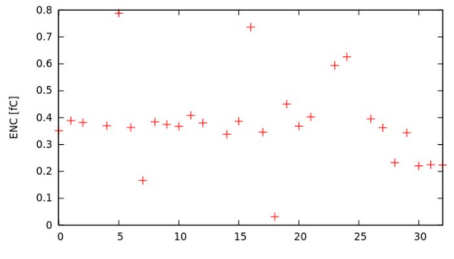


Chip-2









Chip-3

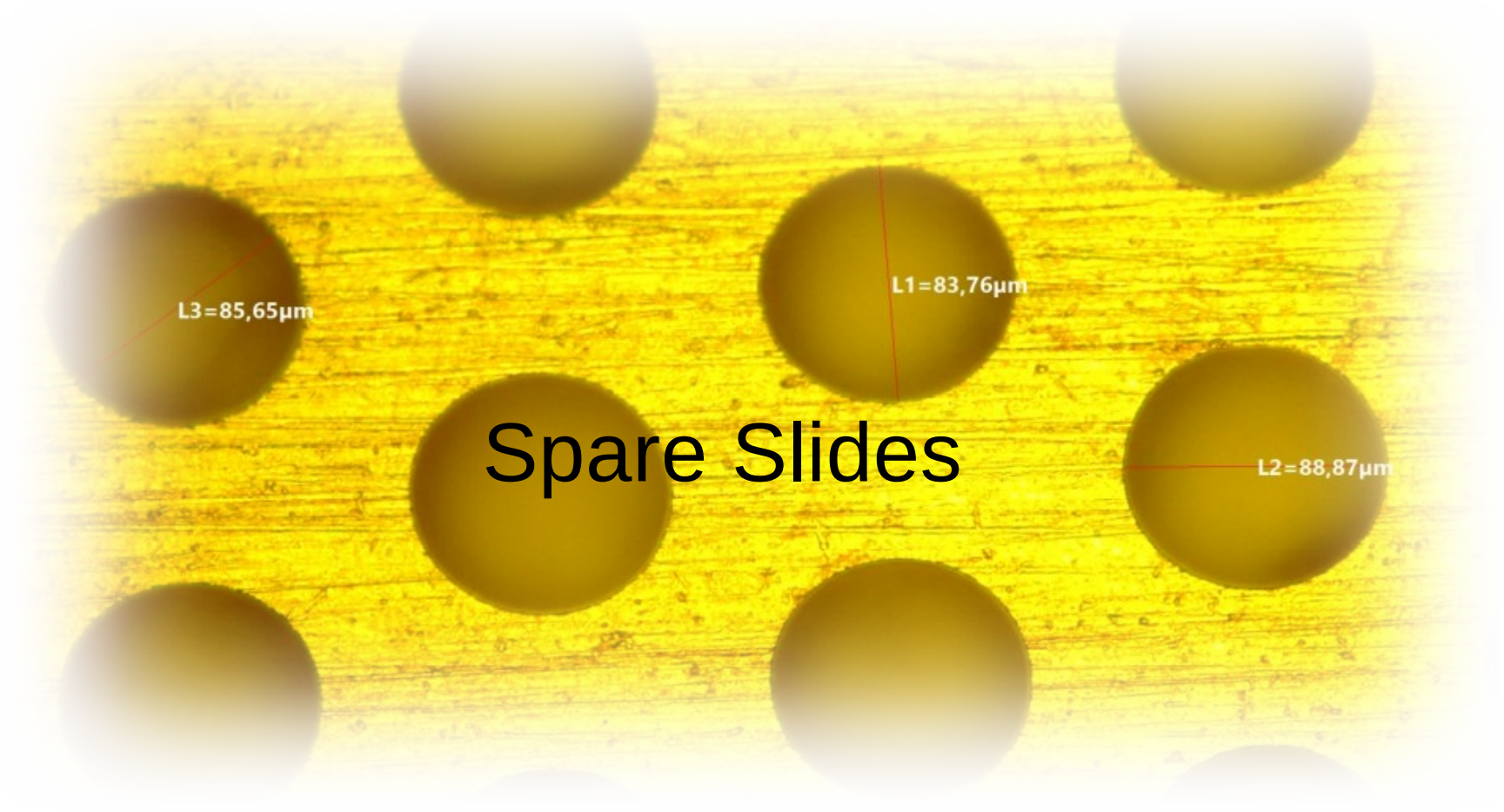
Summary & Outlook

The advances in the **μ-RWELL technology** during the last two years lead to **large improvements** in **terms of stability** and **production yield**

- The challenge for the next two years is the **TT of resistive-MPGD** to the PCB industry (ELTOS)
- **Key-point** is the acquisition of the **DLC magnetron sputtering machine co-funded by CERN and INFN** that is going in operation in these days

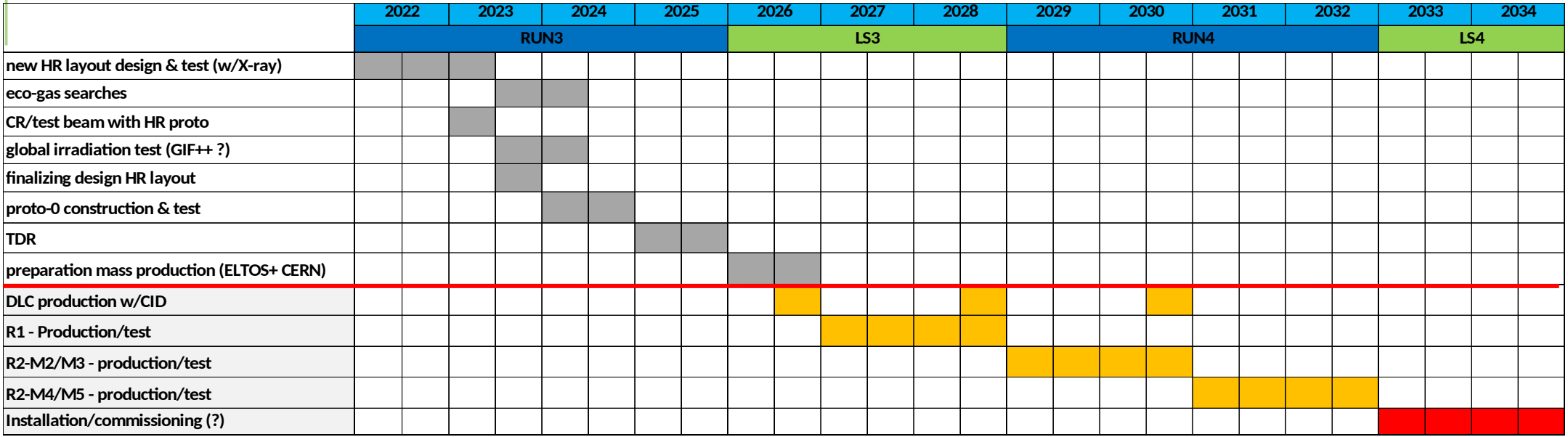
Mid-term To Do List:

- **Integration with the electronics (FATIC)** developed by the **Bari** group, with the goal of a better understanding of the **requirements for a new dedicated ASIC**
- **Test-bench** in Bari for chip validation
- **cosmic ray stand** in Frascati ongoing now
- **Test beam** (eff in 25 ns, OR/maj..etc vs gas mix) within **summer 2023**
- **Optimization** of the **PEP** layout & design of the **M2R1/R2 proto-0 ►2023/24**
- **Global irradiation** (LNF X-ray tube, GIF++ w/Gas CERN group) **►2023/2024**
- **Eco-gas fast** mixtures (to decide...)



Spare Slides

Tentative schedule (2022-2032)



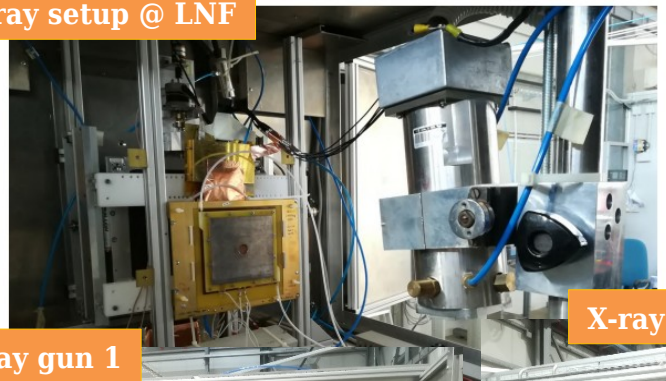
La costruzione segue i seguenti step(*):

- CERN ▭ produzione DLC con macchina sputtering CID
- Eltos ▭ PCB, DLC patterning & gluing
- CERN ▭ finalizzazione rivelatore con etching kapton (RUI)
- CERN ▭ assemblaggio con frame e catodi e procedura di conditioning (RUI)
- CERN ▭ test finale rivelatori e integrazione elettronica (personale INFN)

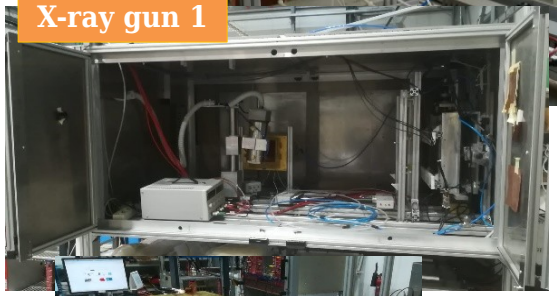
(*) **tempi e modalità di produzione definite con Rui & Eltos e considerando un solo «integration group»**

Test facilities and synergies

X-ray setup @ LNF



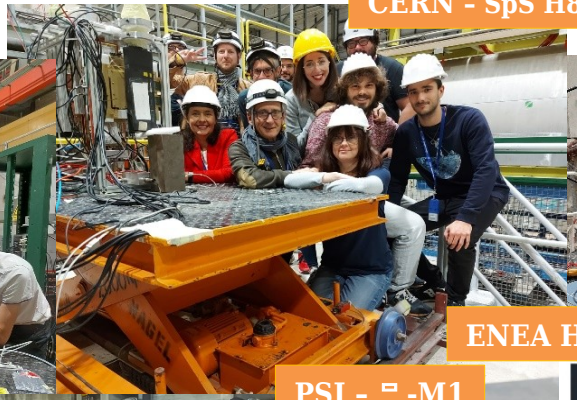
X-ray gun 1

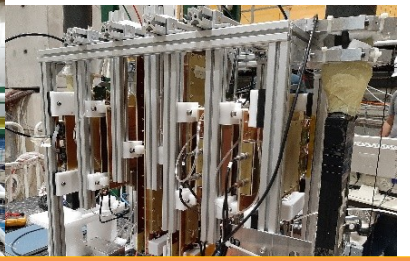


X-ray gun 2

Cosmic ray setup @ LNF

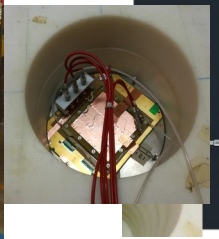
CERN - SpS H8C

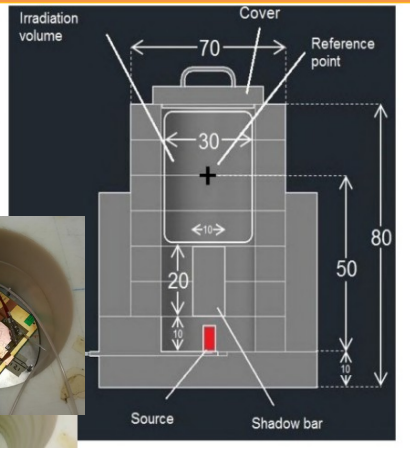




ENEA HOTNES thermal neutron facility

PSI - π -M1





Several **test facilities** in Frascati (LNF/ENEA), CERN (H8C) and PSI (PiM1) are exploited for detectors characterization. **Synergies** with external groups (Ferrara, Bologna, RM2-CLAS12) gave an important boost to the technology. For sure the involvement of other LHCb-Muon groups would be desirable in the near future, in particular in view of the phase of major commitment for the integration tests.

Technology transfer (II)

Step 0 - Detector PCB design @ **LNF**

Step 1 - CERN_INFN DLC sputtering machine @ **CERN**
- Installed and commissioned beginning of Nov 2022
- **Operated by CERN + LNF (& INFN) staff**

Step 2 - Producing readout PCB by **ELTOS**
- pad/strip readout

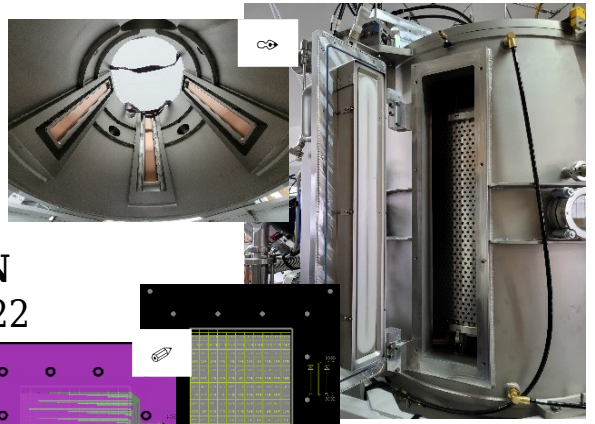
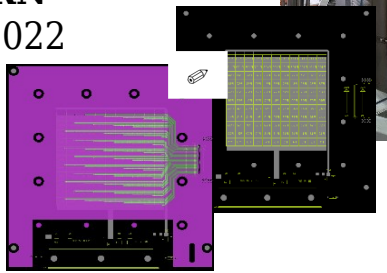
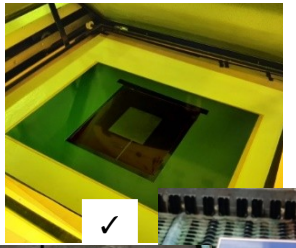
Step 3 - DLC patterning by **ELTOS**
- photo-resist = patterning with BRUSHING-machine

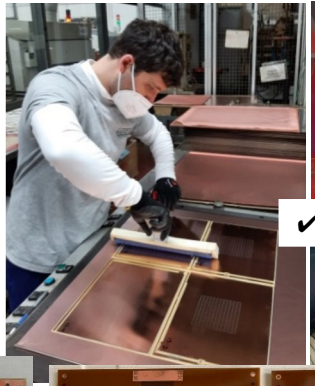
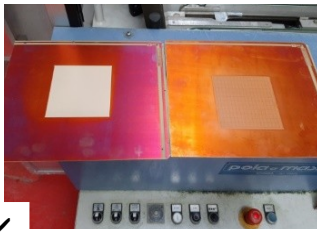
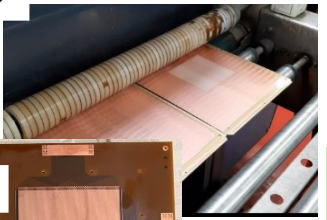
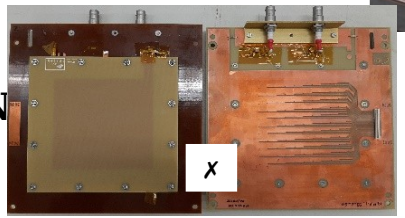
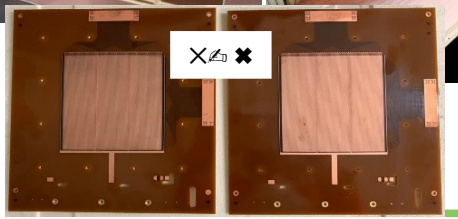
Step 4 - DLC foil gluing on PCB by **ELTOS**
- double 106-prepreg ~ 2x50 µm thick
- PCB planarizing w/ screen printed epoxy = single 106-prepreg

Step 5 - Top copper patterning by **CERN** (in future by **ELTOS)**
- Holes image and HV connections by Cu etching

Step 6 - Amplification stage patterning by **CERN**
- PI etching = plating = ampl-holes

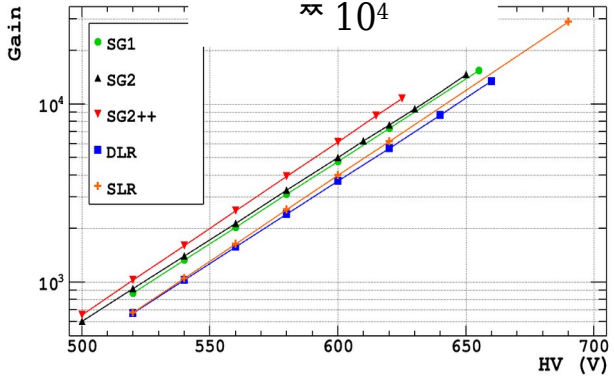
Step 7 – Final electrical cleaning and detector closing @ **CERN**

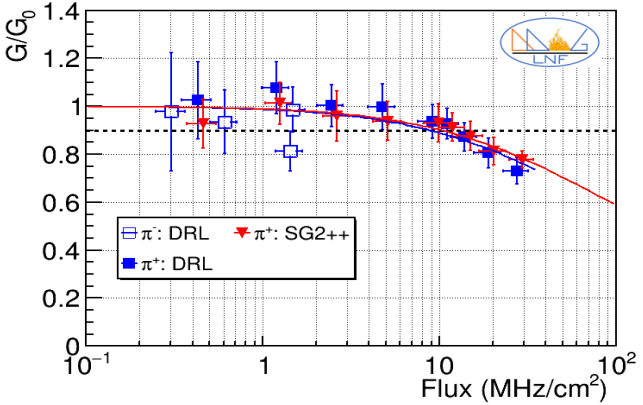







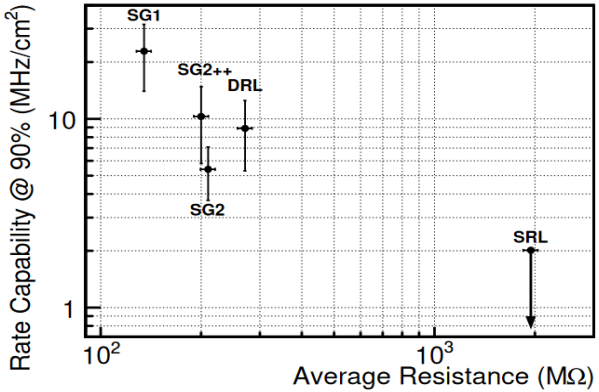
High-rate layouts performance w/m.i.p.

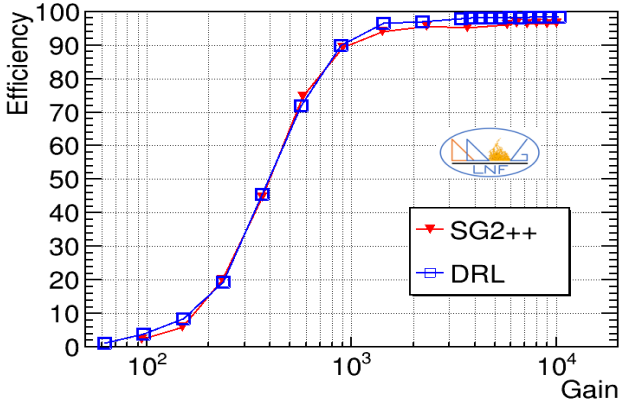
Gain up to ≃ 10^4



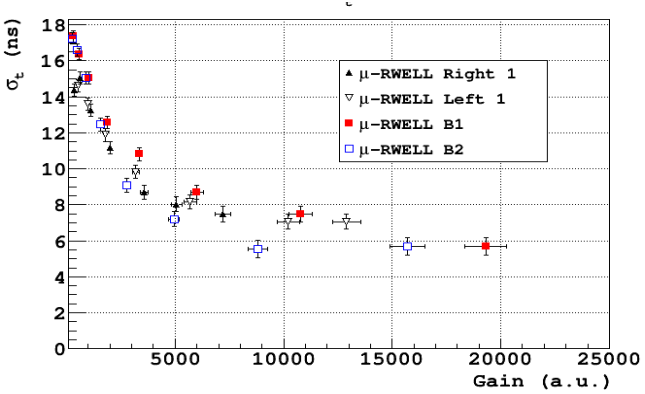
Rate capability up to 10 –20 MHz/cm^2



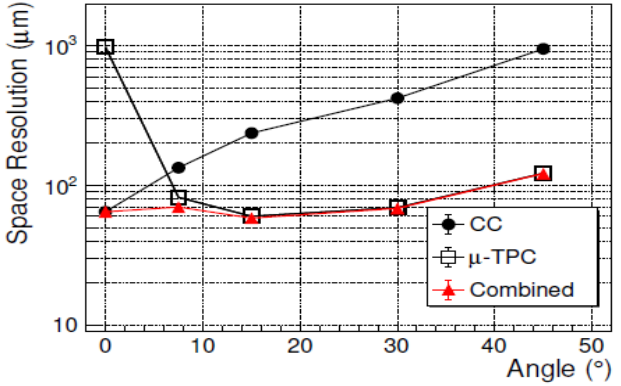




Efficiency ≃ 97%



Time resolution 5-6 ns

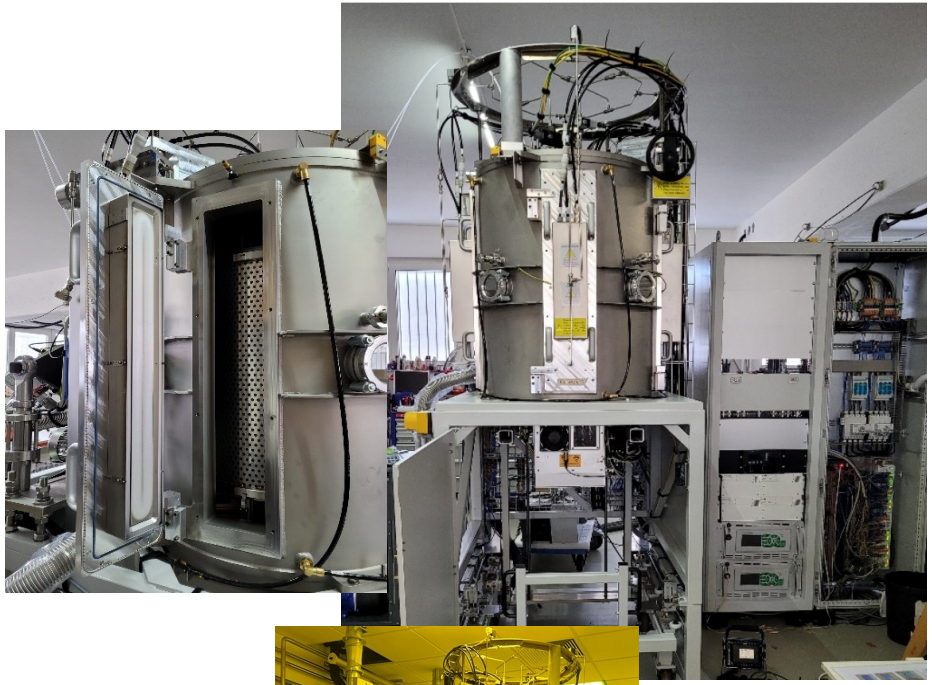


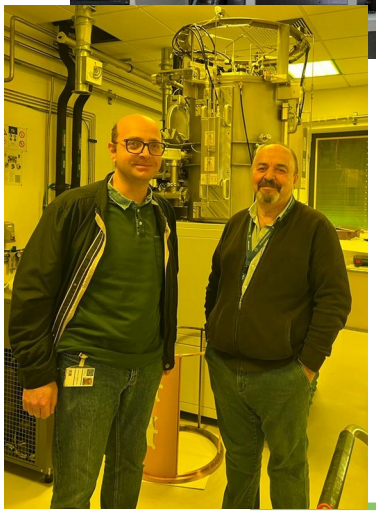
Space resolution down to 60 μm

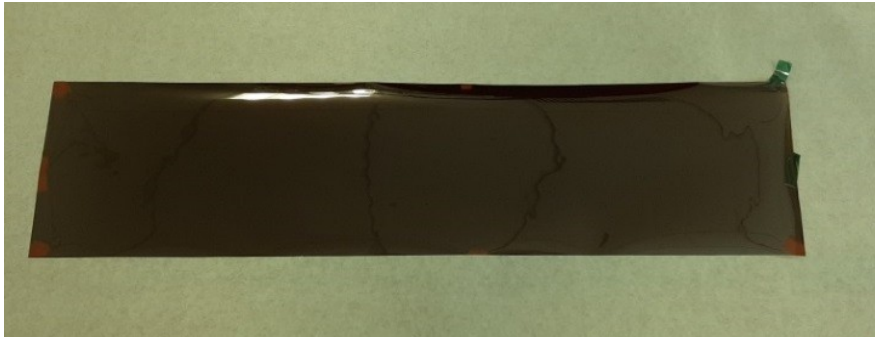
The micro-RWELL layouts for high particle rate, G. Bencivenni et al., 2019 JINST 14 P05014

CID: the CERN-INFN DLC machine

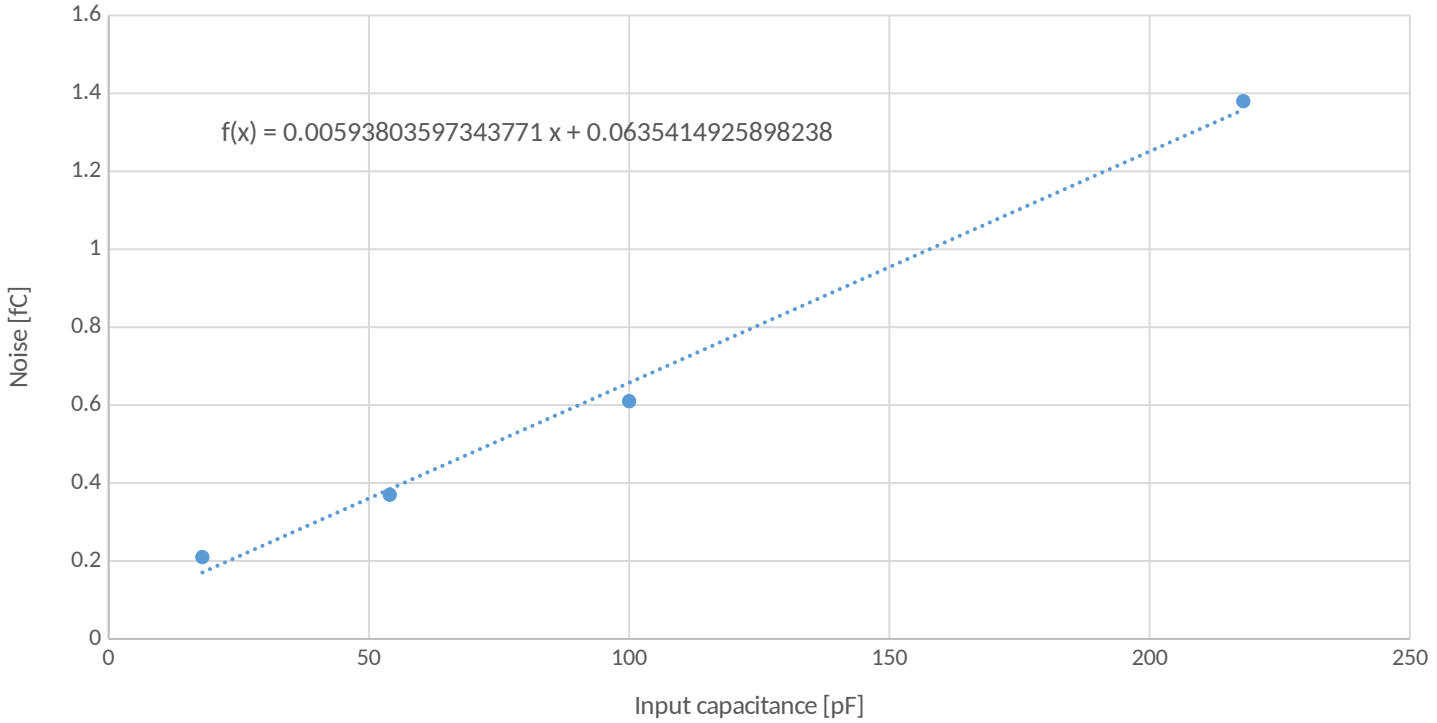
- **Flexible substrates, coating** areas **up to 1.7 m × 0.6 m**
- **Rigid substrates, coating** areas up to **0.2 m × 0.6 m**
- **Five cooled target holders,** arranged as two pairs face to face and one on the front, equipped with five shutters
- **Sputtering & co-sputtering different materials,** in order to create a coating layer by layer or an adjustable gradient in the coating





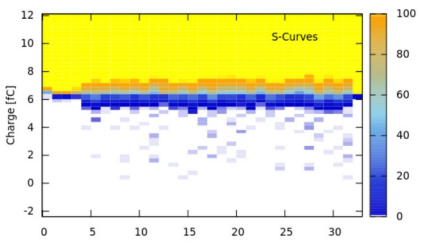


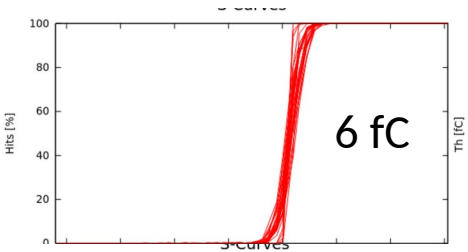
Measure: CSA noise vs input capacitance

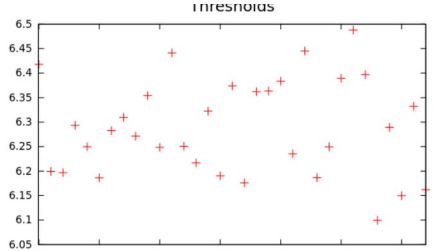


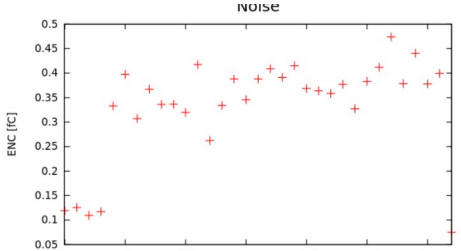
Measurement conditions: fast-branch, LG, positive polarity

Measure: fast discriminator

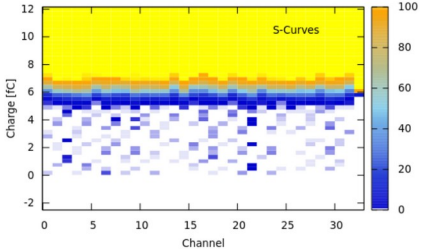


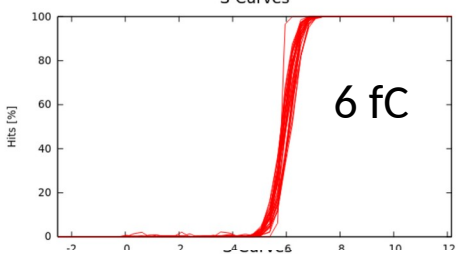


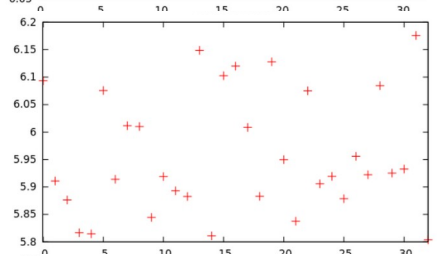


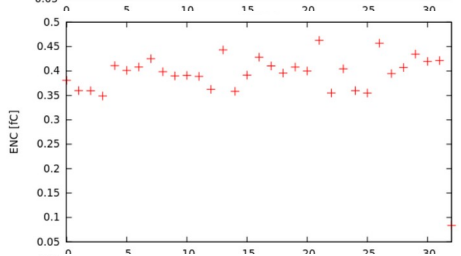


Chip-0

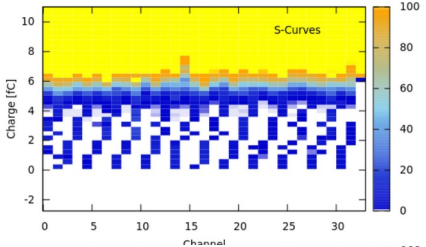


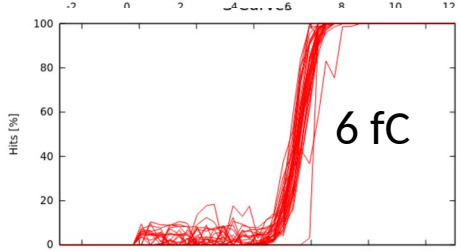


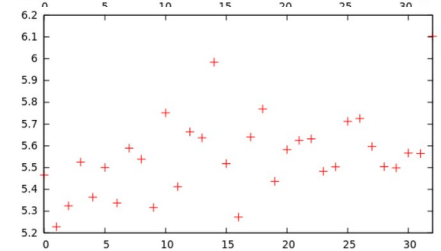


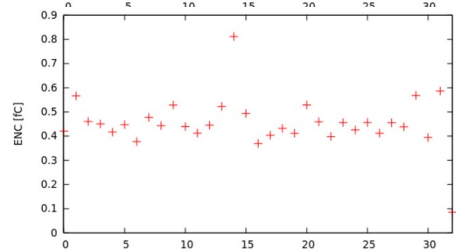


Chip-1

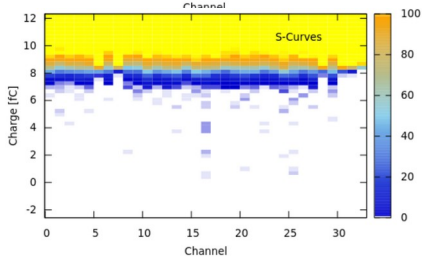


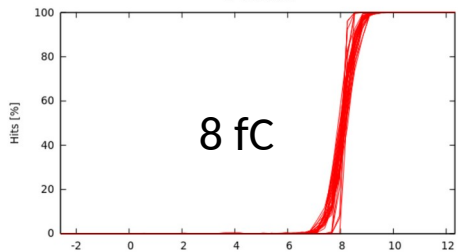


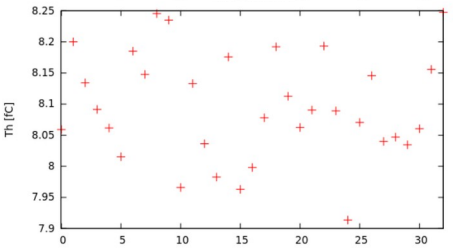


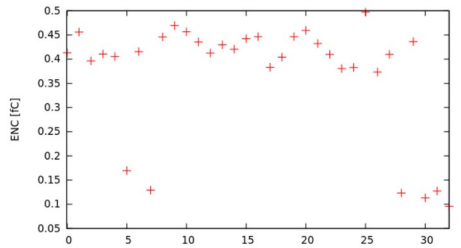


Chip-2



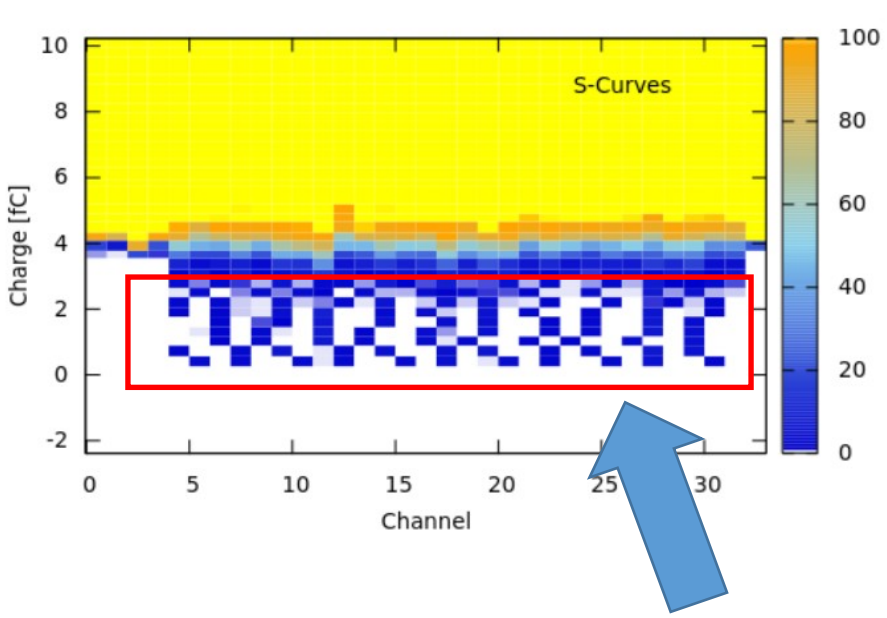


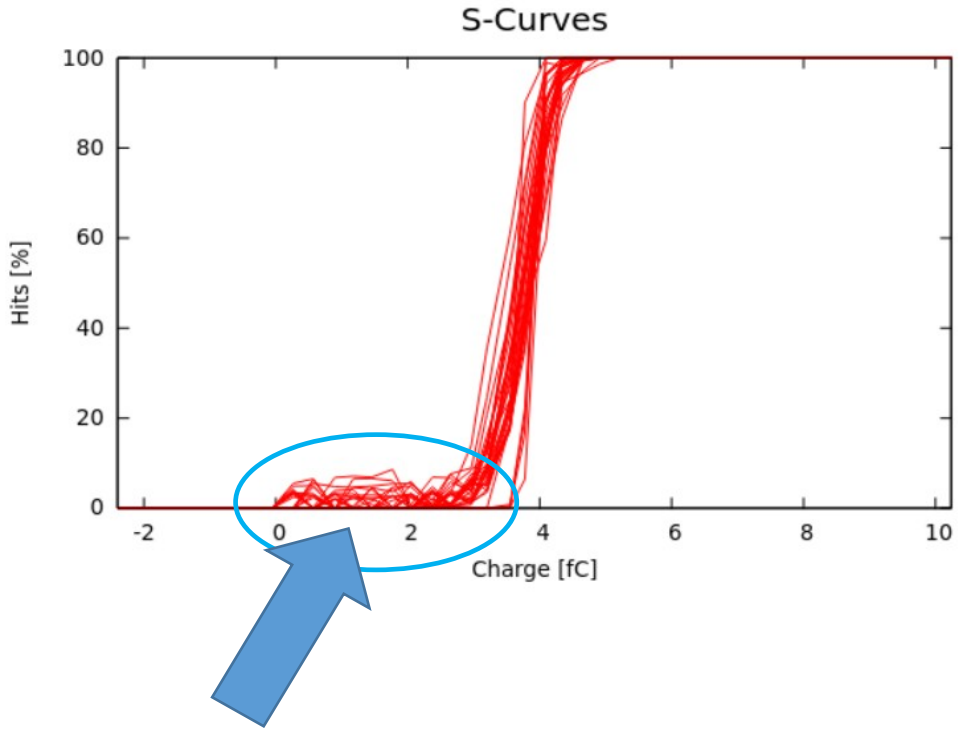




Chip-3

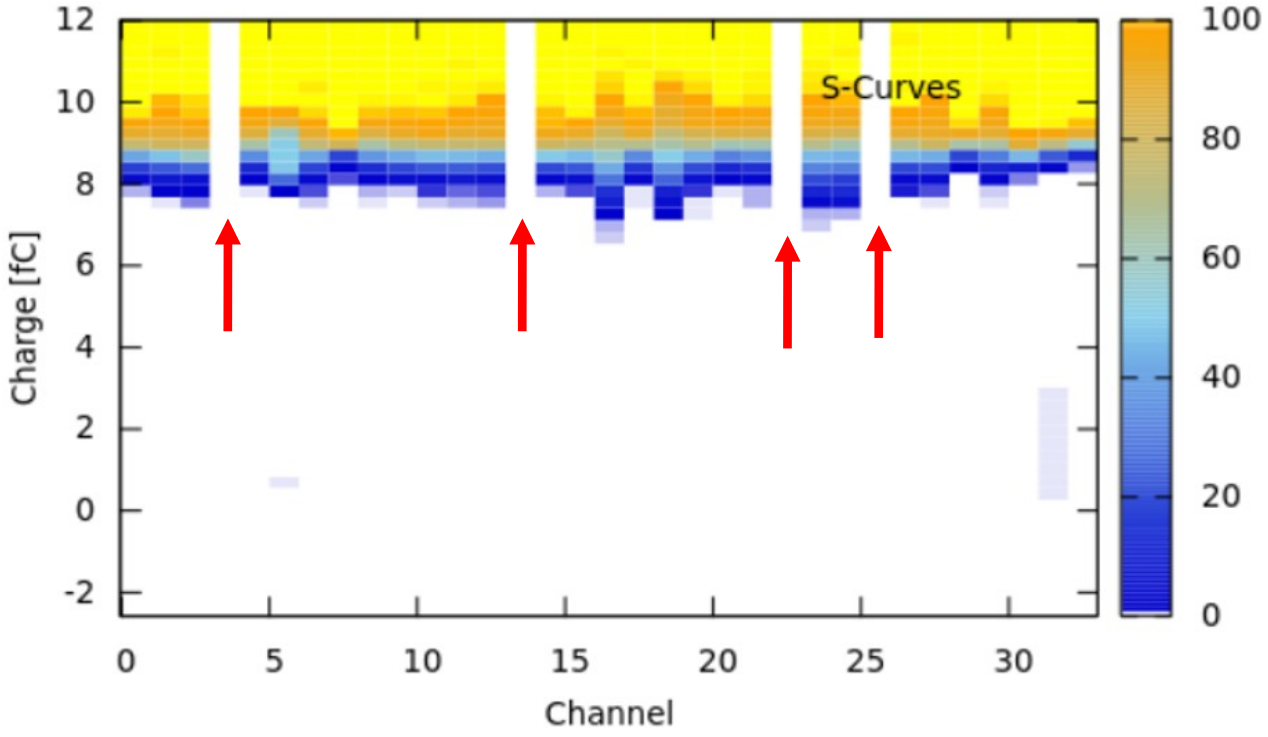
Non gaussian noise





This noise should not present in a system effected only by gaussian noise (electronic noise)

Stucked channels



In this scan:
4 channels stucked before scan

A know bug in the channel FSM is triggered by the noise.
When channel is stucked, the only way to recover is an hard reset.

Firmware and software

Firmware is based on the MOSAIC architecture

- Data transfer @320 Mbps from each FATIC2 chips
- Data filter to emulate triggered acquisition
- Board memory buffer - 1 GB
- Ethernet sustained data transfer 120 MBps (~1 Gbps)

Current software is able to perform all hardware related tasks:

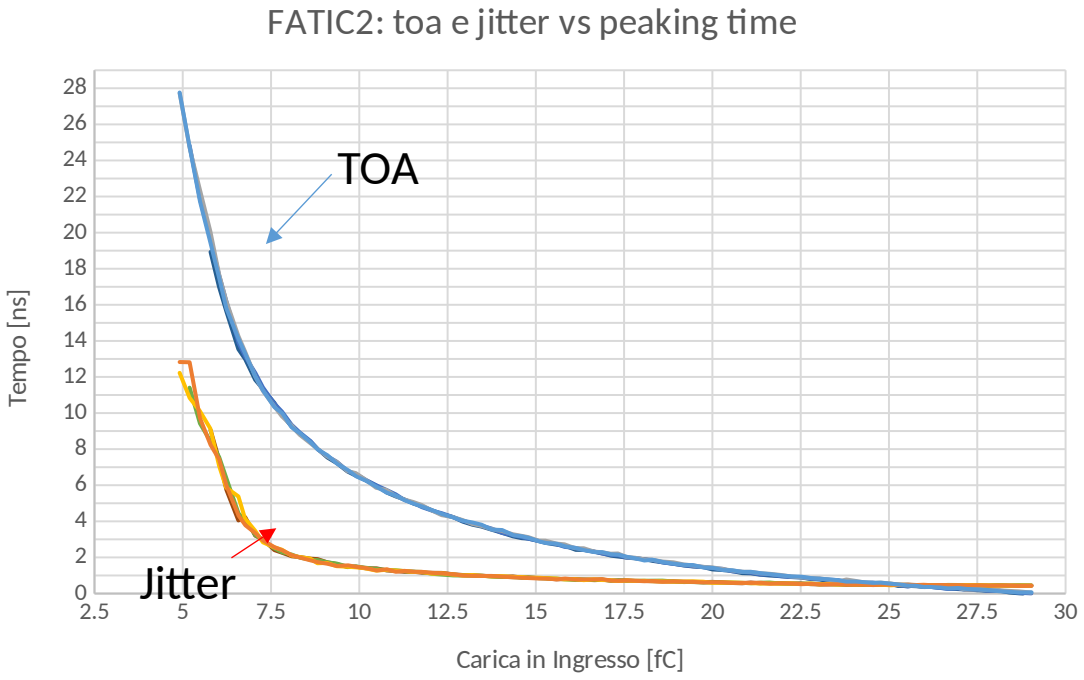
- DAQ Board + FATIC2 chips configuration
- Equalize channel discriminator thresholds
- Charge scan => S-curves, Hit-maps, Effective thresholds, Noise
- Data acquisition

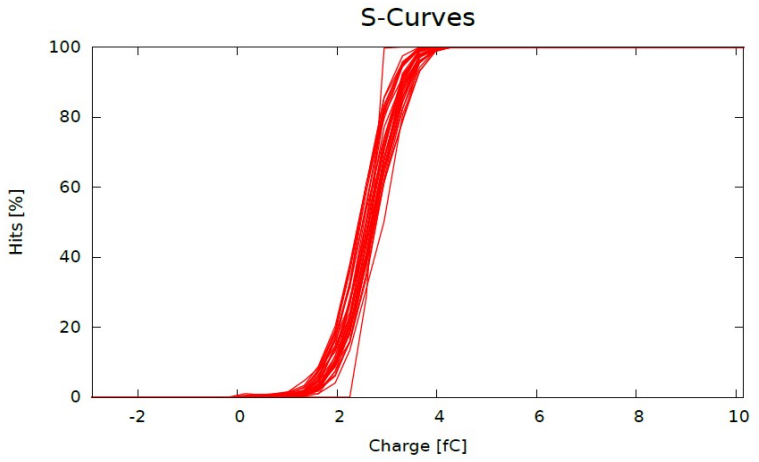
To do

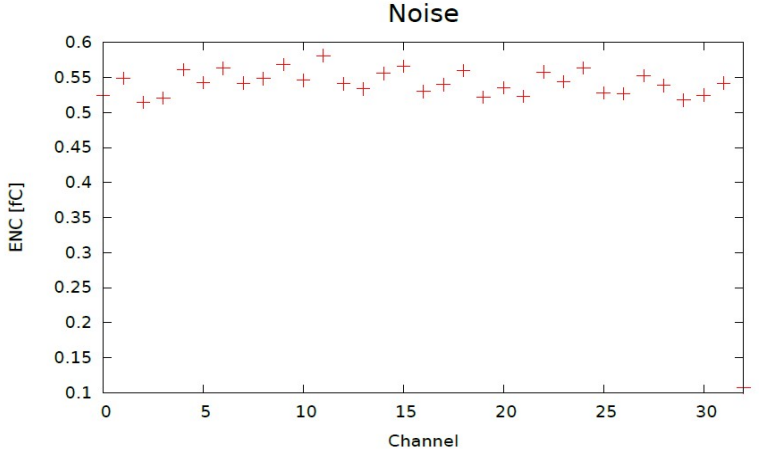
- INFN-Bari:
  - Enable MOSAIC firmware to read 4 Front-end boards
  - Wire bonding of 6 additional FEBs and test
  - Implement multi-board synchronization, configuration and readout

- Test @ INFN-Frascati:
  - 10 x 10 cm2 u-rwell + FATIC2_FEB, FATIC2 test board
  - Measurement with cosmic muons
  - Test target:
    - Timing measurements (with FATIC2_FEB)
    - Charge measurements (with FATIC2_FEB): statistic on the u-Rwell charge

Fast-branch: timing measurements

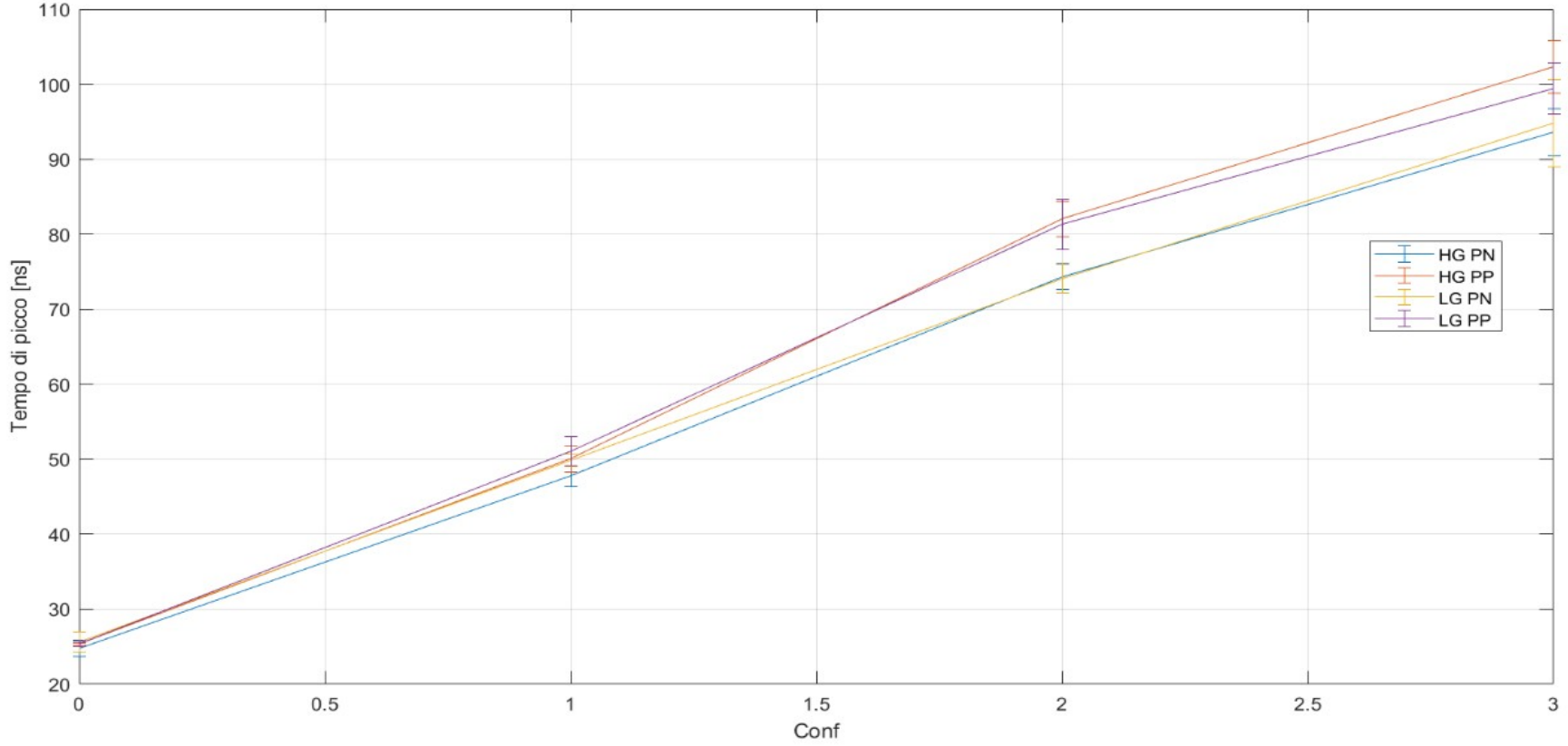




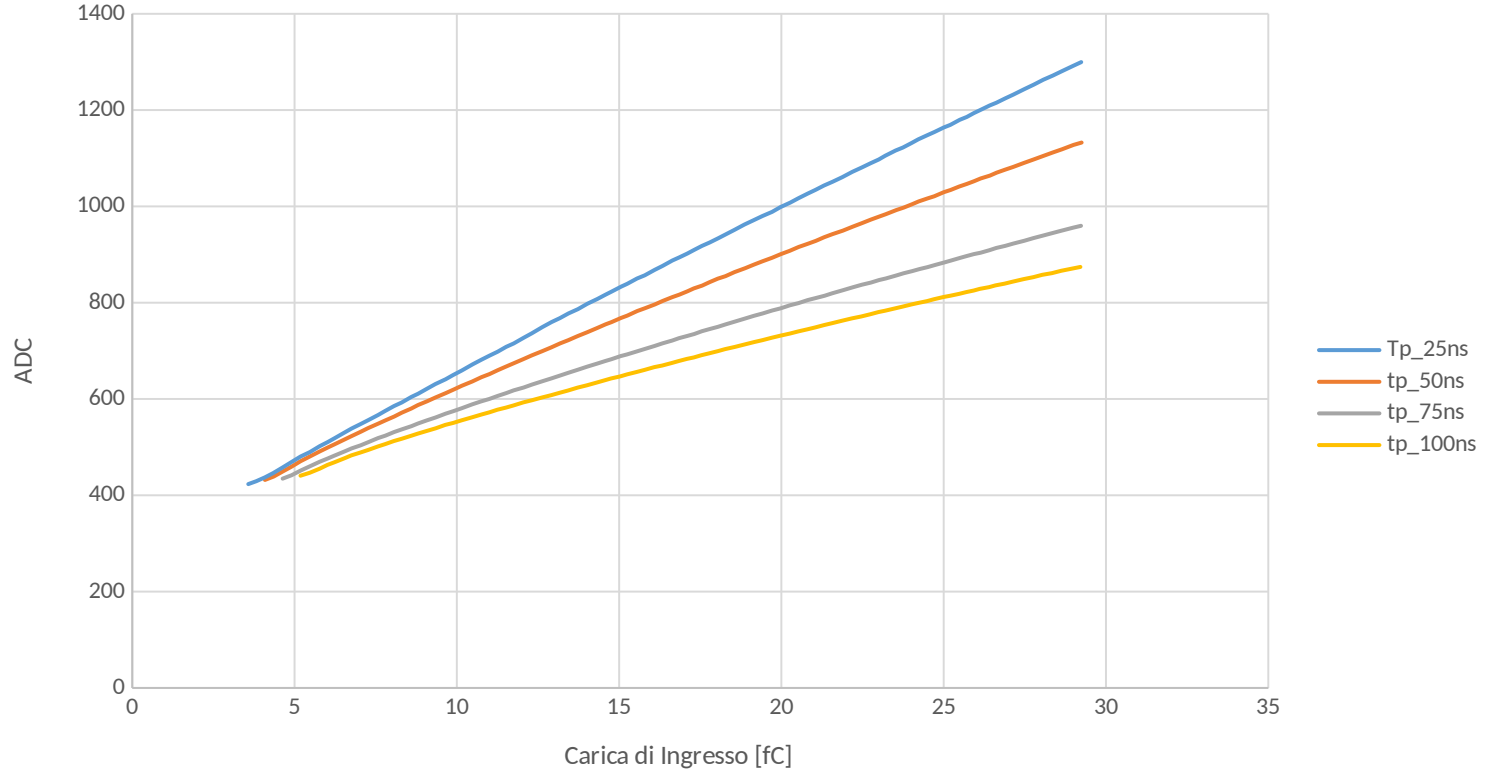


Measurement conditions: fast-branch, LG, positive polarity, 100 pF input capacitance, threshold 4.5 fC

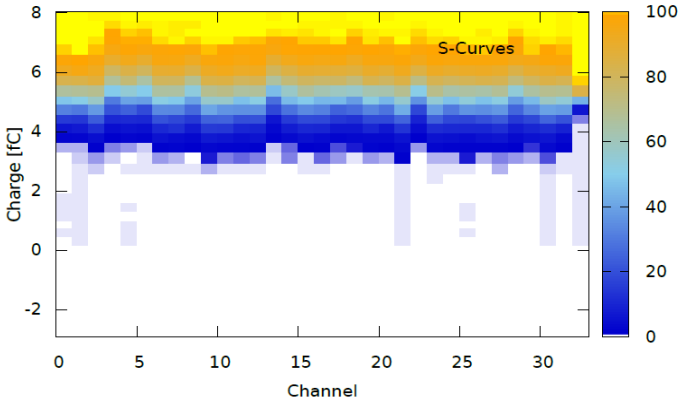
Charge branch: peaking time measurement

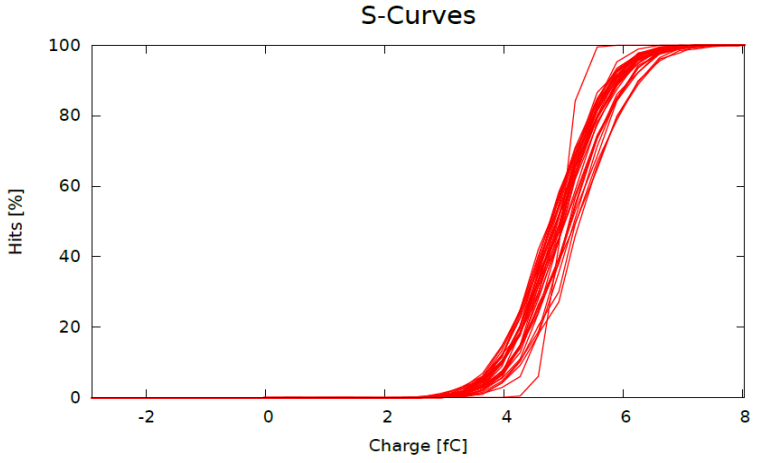


Charge branch: charge measurement



Scan with only gaussian noise (Different setup)





Operating condition:
Cin = 100 pF
Theshold = ~5 fC
ENC = ~0.75 fC