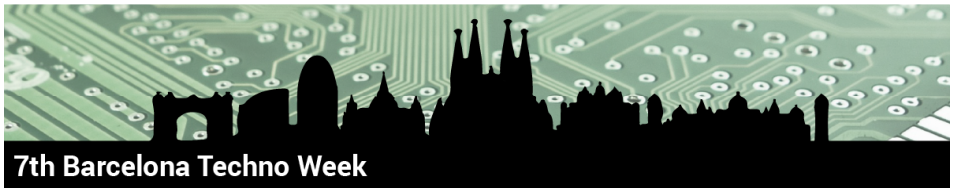

Contribution ID: **24** Type: **Contributed e-poster**

Model and analysis of the future ALICE ITS3 wafer-scale on-chip readout architecture

Thursday, July 6, 2023 4:35 PM (1h 25m)

The ALICE collaboration is developing the Inner Tracker System 3 (ITS3), a novel detector that exploits the novel stitching technique to construct cylindrical single-die monolithic pixel sensors of up to 266 mm x 93 mm. ITS3 requires all hits from a particle flux of 4.4 MHz/cm2 to be transmitted on-chip to one of the sensor edges with a readout inefficiency of <0.1 % of hits lost while keeping a power consumption budget of 20 mW/cm2 and a dead area ≤10 %. The objective of this work is to carefully dimension the different components of this on-chip readout architecture adjusting it to the requirements and constraints of the ITS3. To do so, a model of the on-chip architecture was developed using System Verilog. This model provided different readout performances under different parameter configurations, readout architectures, and data inputs. Apart from this, it provided key learnings for the readout architecture implementation such as the correlation between losses and collisions pile-up, or the best ordering for reading the memories. From this model, it was observed that ~3 on-chip data lines/cm2 of ~160 Mbit/s each and ~13 memories/cm2 of ~64 words depth each were sufficient to cope with the requirements.

Primary author: VIQUEIRA RODRIGUEZ, Manuel (CERN)

Presenter: VIQUEIRA RODRIGUEZ, Manuel (CERN)