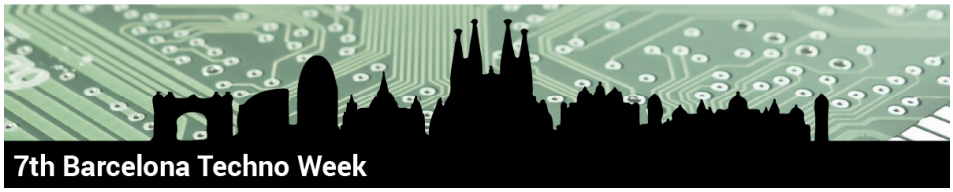

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Pix-ESL: a SystemC framework for architectural modelling of readout systems in HEP

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The high cost of prototyping at advanced technology nodes, as well as the complexity of future detectors, necessitate the use of a system design technique widely used in industry: design space exploration through high-level architecture studies to establish
precise and optimal requirements. This work presents Pix-ESL: a programmable SystemC framework for simulating the readout chain from the front-end chips to the detector back-end. The model is transaction accurate, comprises an event generator and
connects with real-world physics events, and provides metrics such as readout efficiency, latency, and average queue occupancy. This contribution outlines the framework's structure as well as a case study based on Velopix2.

Primary author: DHALIWAL, Jashandeep (CERN)

Co-authors: Mr CERESA, Davide; Mr BRAMBILLA, Francesco Enrico; Mr ESPOSITO, Stefano