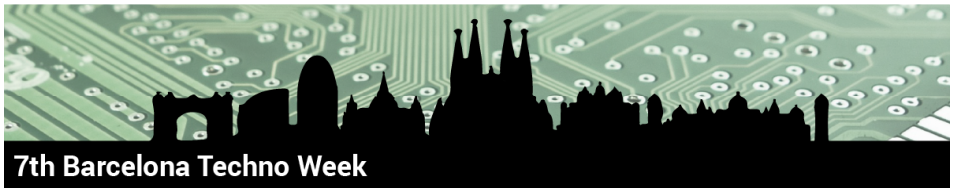

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A Scalable Frame-Based Readout Architecture for Monolithic Pixel Detectors with Local ADC and Time Digitization

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We proposes a novel readout architecture for monolithic pixel sensors for photon and particle detection, capable of handling event rates on the order of tens of kilohertz, while maintaining accurate timing resolution and energy deposition measurements. Our solution involves a scalable and versatile architecture with a local ADC integrated outside the pixels, but within the active-matrix area. Pixels are organized in a macro block, "super-pixel", that acts as a standalone data processing unit, and sends data on a serial bus at 200 MHz. The integration of multiple super-pixels in parallel optimizes readout time for larger matrices, thanks to a distributed digital logic and local charge measurement. This architecture has been applied to the development of the ASIC in a 130 nm SiGe BiCMOS technology for the FASER pre-shower detector at CERN, proving this concept on silicon.

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