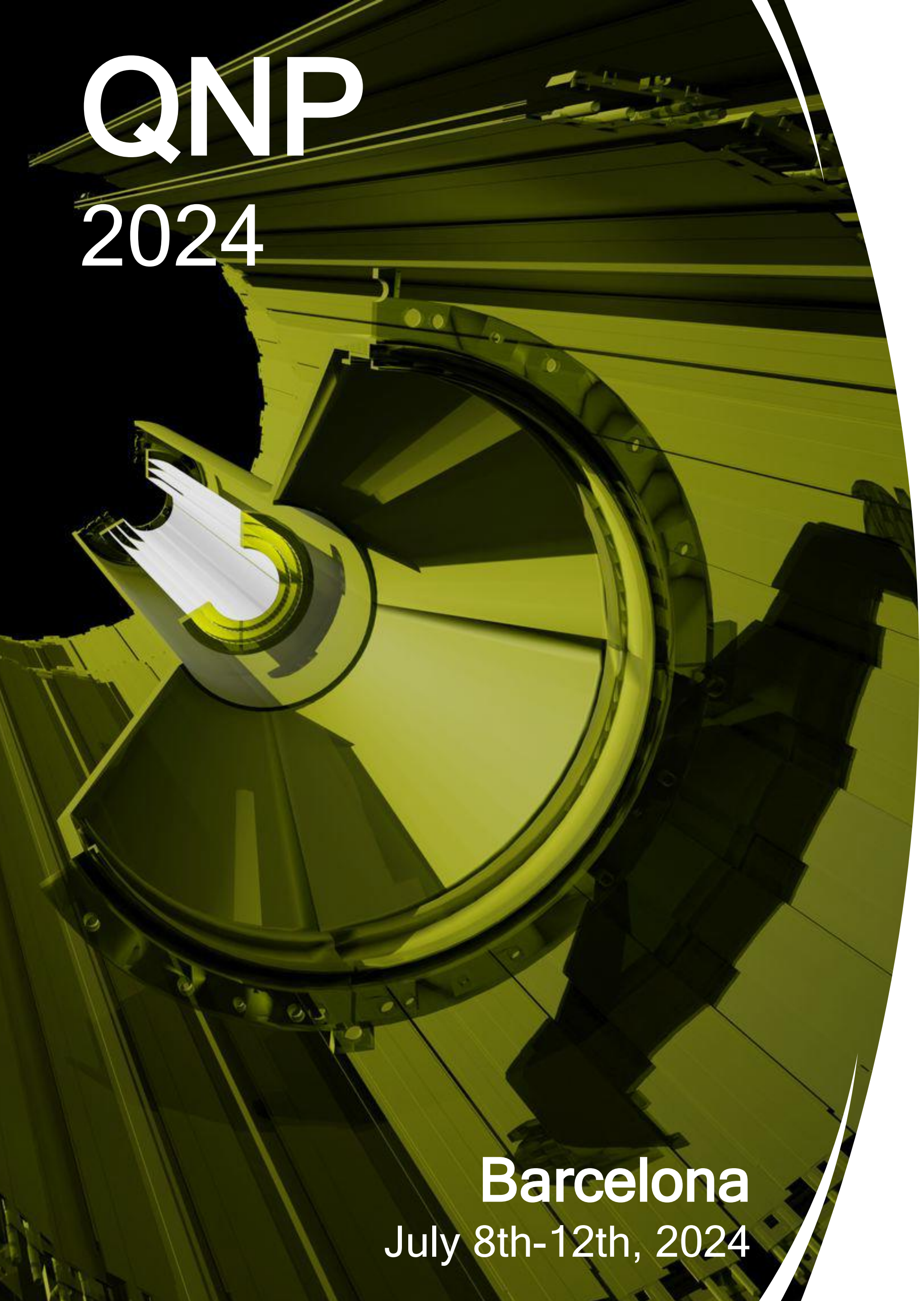


QNP
2024

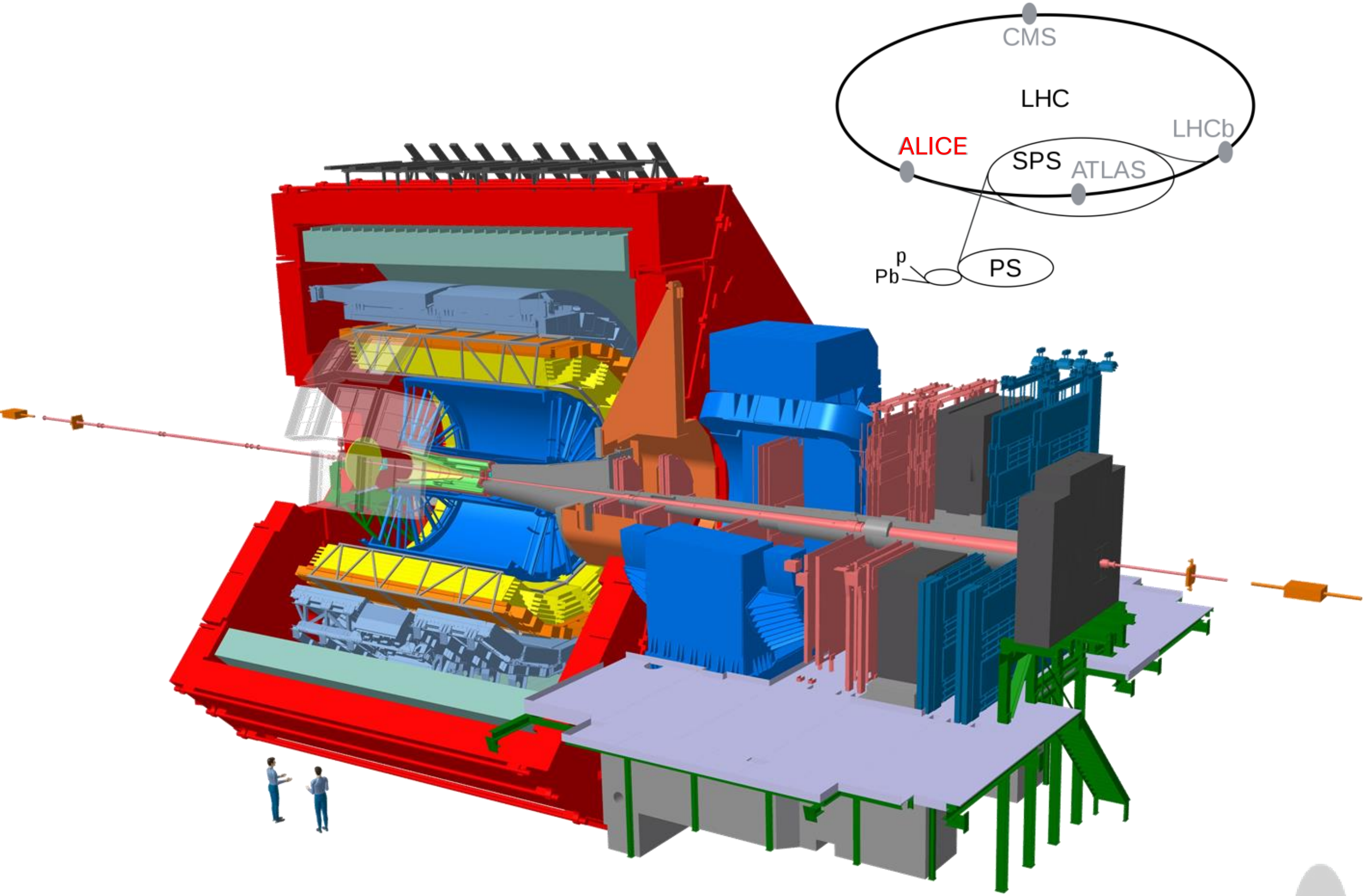
Barcelona
July 8th-12th, 2024

ITS3: the next upgrade of the ALICE Inner Tracking System

Paola La Rocca
INFN and University Catania

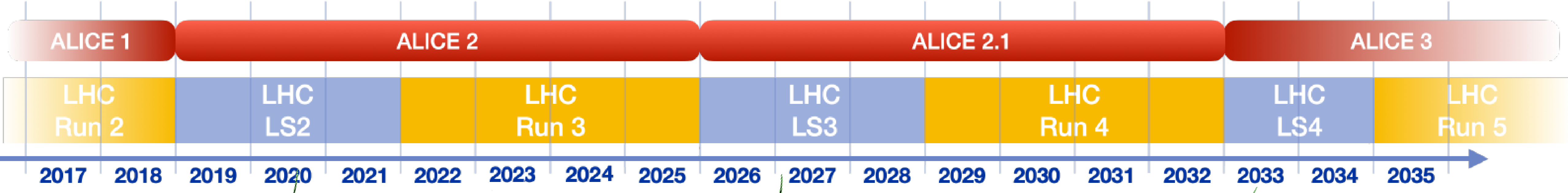
on behalf of the ALICE Collaboration

The ALICE experiment

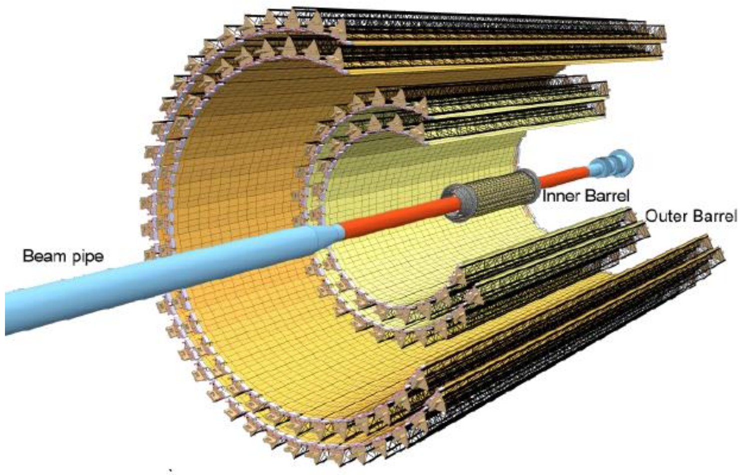


- Study of strongly interacting matter at extreme densities (QGP) in heavy ion collisions at the LHC (CERN)
- Very high multiplicities tracking of up to O(10k) particles in single event
- Reconstruction of charm and beauty hadrons
- Interest in low momentum ($\lesssim$1 GeV/c) particle reconstruction

ALICE silicon tracker development timeline

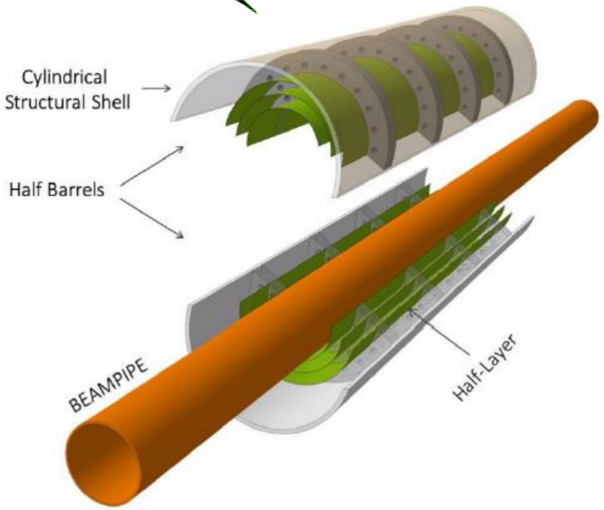

ALICE 1
ALICE 2
ALICE 2.1
ALICE 3
LHC Run 2
LHC LS2
LHC Run 3
LHC LS3
LHC Run 4
LHC LS4
LHC Run 5
2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035

ITS2



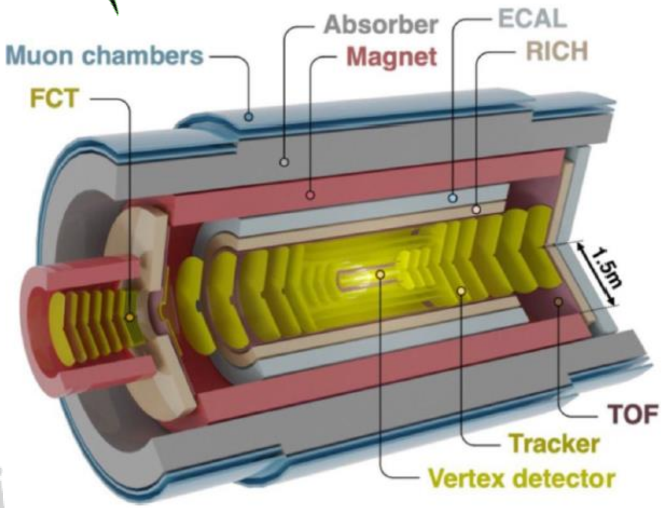
S. Acharya et al 2024 JINST 19 P05062

ITS3



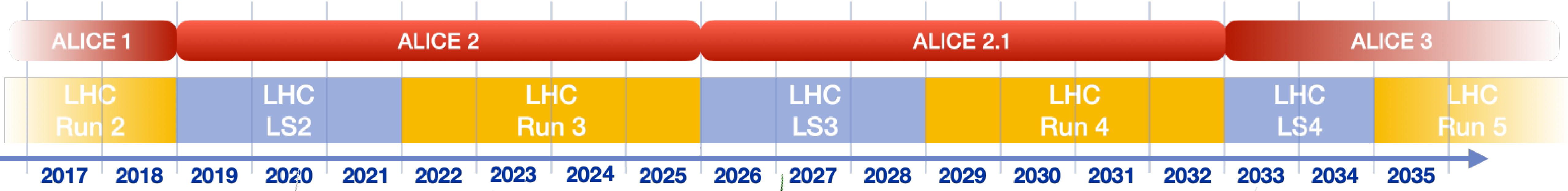
LOI: CERN-LHCC-2019-018
TDR: CERN-LHCC-2024-003

ALICE3



LOI: CERN-LHCC-2022-009
Scoping Document in preparation

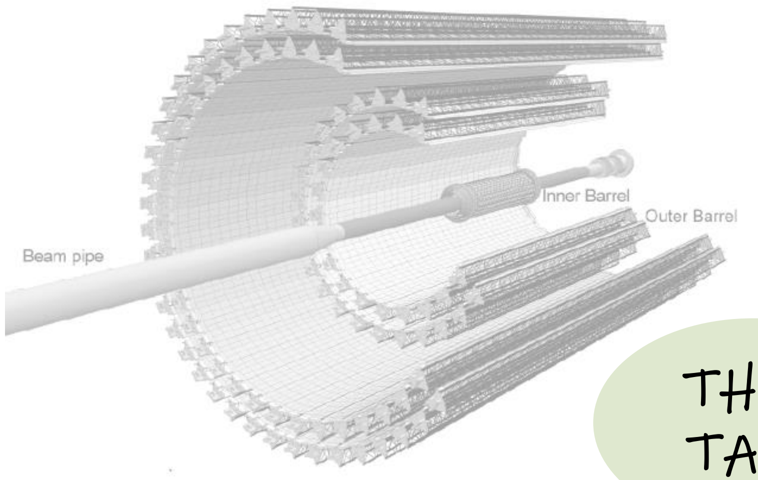
ALICE silicon tracker development timeline


ALICE 1 | ALICE 2 | ALICE 2.1 | ALICE 3

LHC Run 2 | LHC LS2 | LHC Run 3 | LHC LS3 | LHC Run 4 | LHC LS4 | LHC Run 5

2017 2018 2019 2020 2021 2022 2023 2024 2025 2026 2027 2028 2029 2030 2031 2032 2033 2034 2035

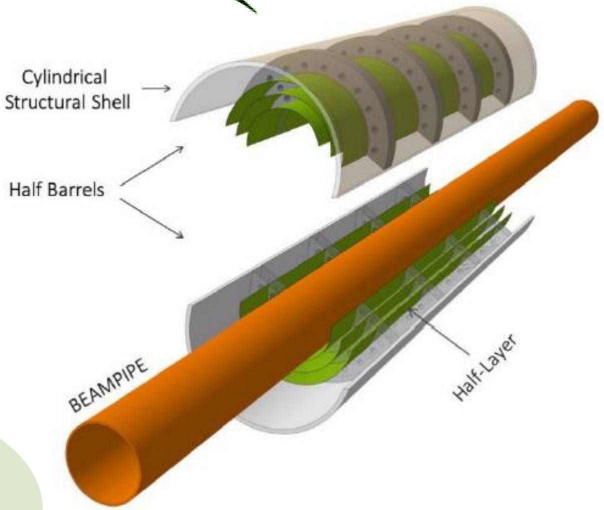
ITS2



S. Acharya et al 2024 JINST 19 P05062

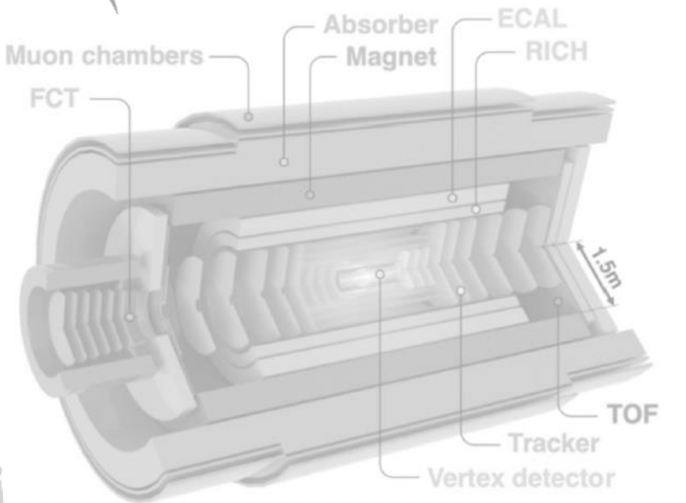
THIS TALK

ITS3



LOI: CERN-LHCC-2019-018
TDR: CERN-LHCC-2024-003

ALICE3



LOI:CERN-LHCC-2022-009
Scoping Document in preparation

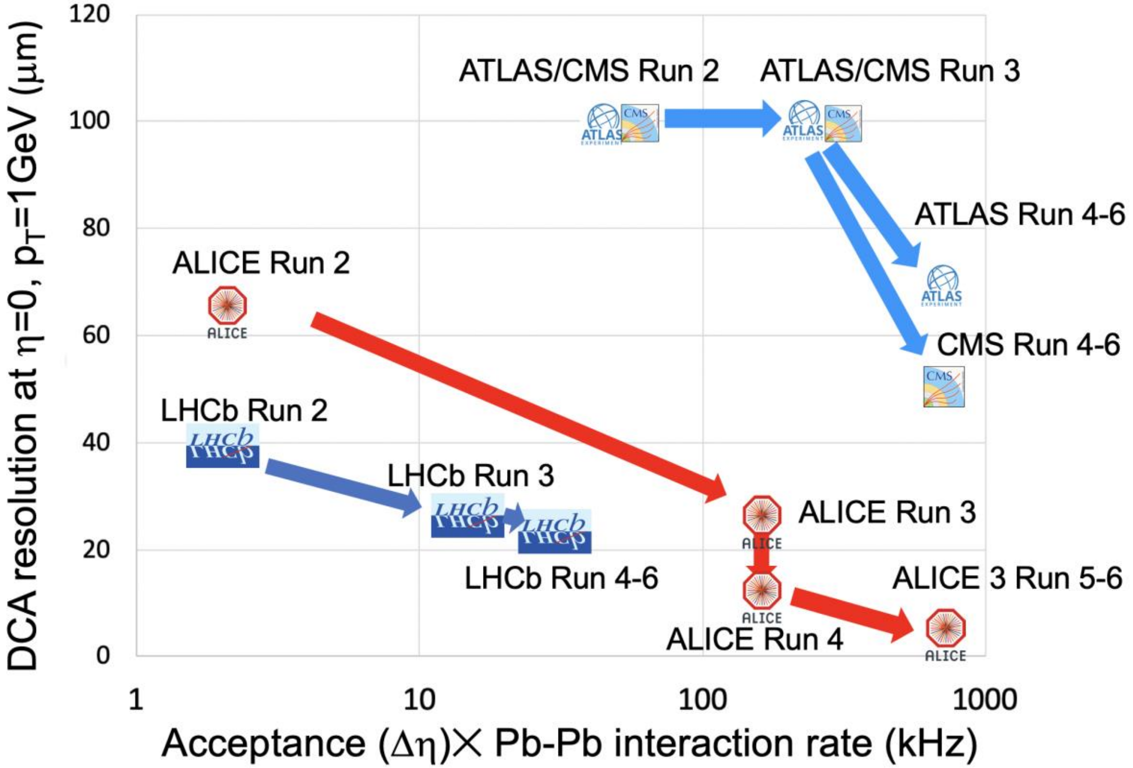
Upgrade motivations and requirements

ALICE 2 → ALICE 2.1

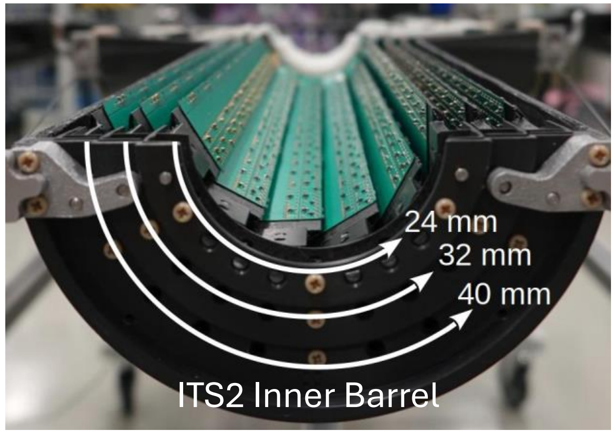
- Impact parameter resolution reduced by a factor of ~2 in low p_T region
- Tracking efficiency up to more than 30% higher, in low p_T region

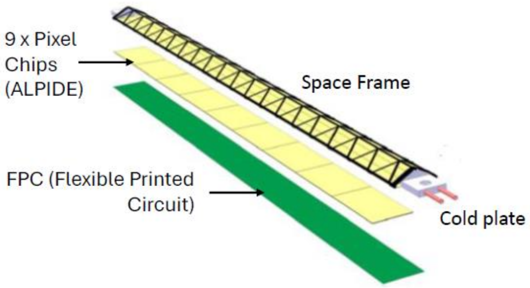
Most striking improvements in the study of:

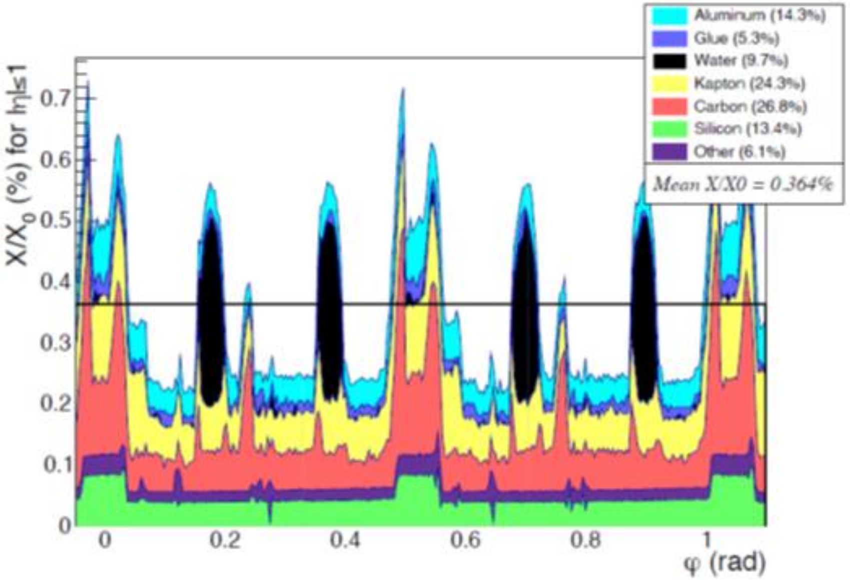
- Low momentum charm and beauty hadrons
- Low-mass dielectrons
- Beauty baryons
- Beauty-stange mesons
- Charm strange and multi-strange baryons
- Light charm hypernuclei



How to improve ITS2







Non-sensitive material

→ Silicon has 1/7 of total material budget

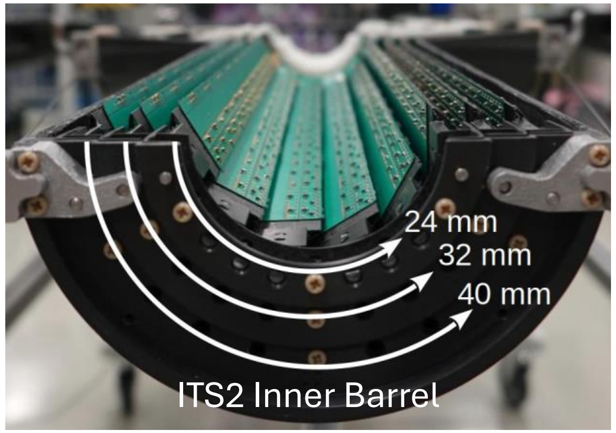
Non-uniformly distributed material

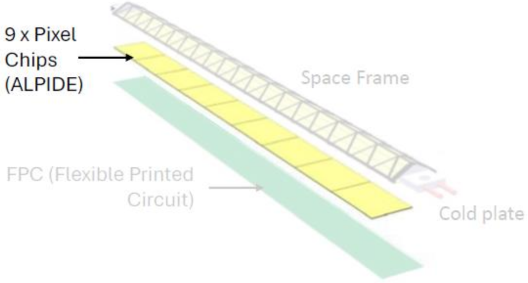
→ Stave overlapping, support and water-cooling structure

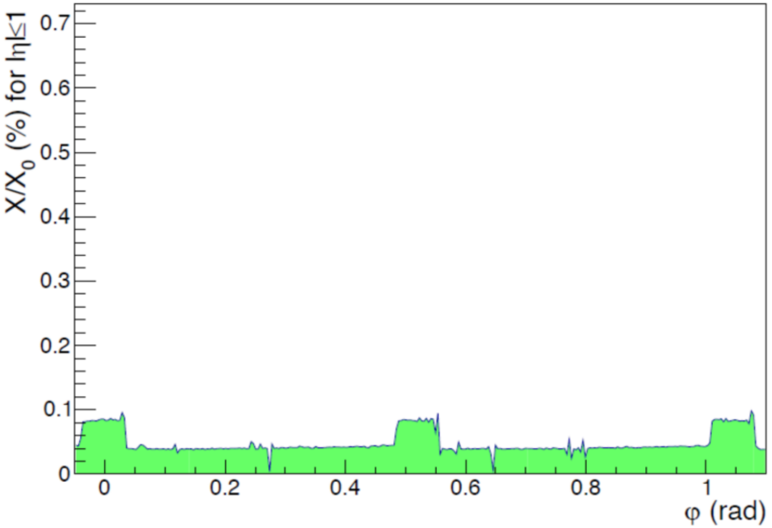
Unable to be closer to the interaction point

→ Mechanical constraints

How to improve ITS2







Non-sensitive material

→ Silicon has 1/7 of total material budget

Non-uniformly distributed material

→ Stave overlapping, support and water-cooling structure

Unable to be closer to the interaction point

→ Mechanical constraints

Removal of water cooling

Possible if power consumption stays below 40 mW/cm^2

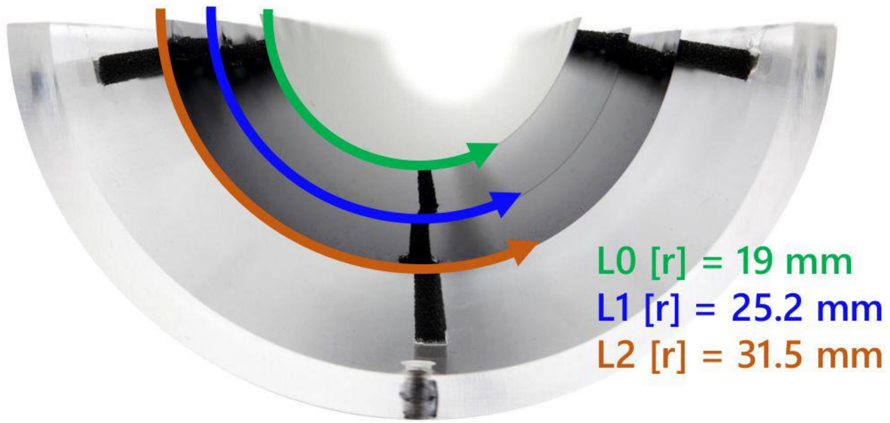
Removal of circuit boards (power and data)

Possible if integrated on Silicon sensors

Removal of mechanical structure

Stability due to bent Silicon wafers

ITS3 - truly cylindrical wafer-scale MAPS



ITS3 Engineering Model 1

LAYOUT:

Replacement of the ITS2 Inner Barrel with 3 layers of **bent wafer-scale sensor ASIC**

Technology:

- **MAPS** in 65 nm CMOS process
- 300 mm **wafer-scale** chips, fabricated using stitching
  → 3 layers with 6 sensors
- Thinned down to 50 µm
  → **Flexible** (bent to target radii)
- Air cooling and ultra-light mechanical supports (carbon foam)

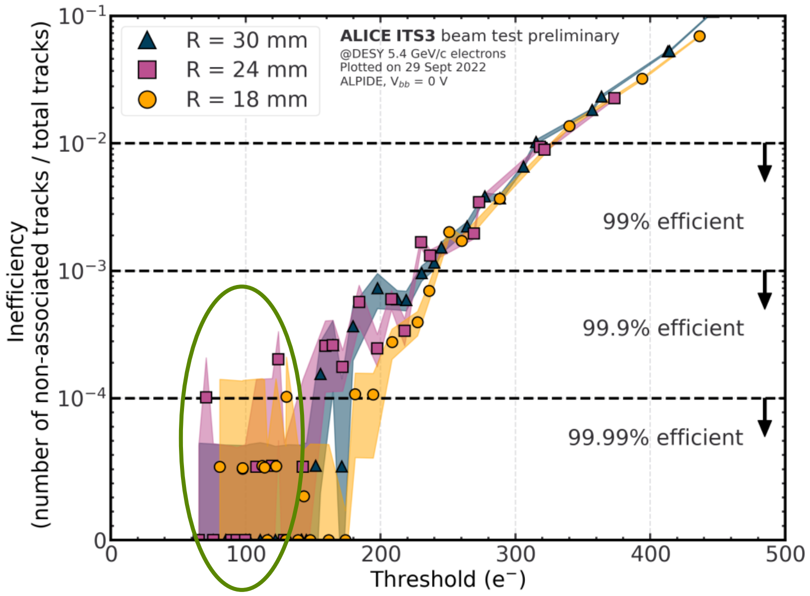
Benefits:

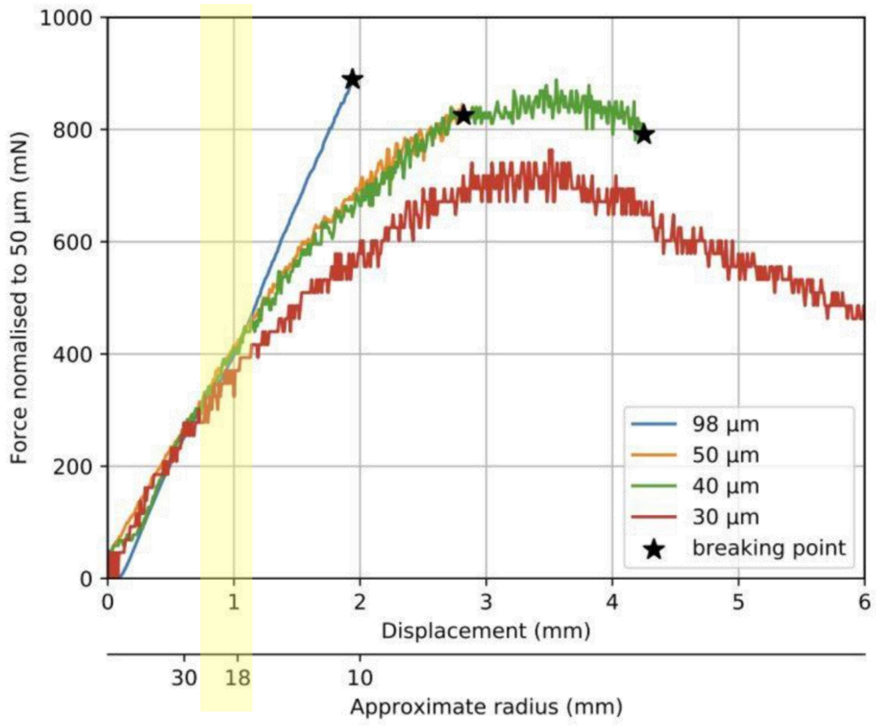
- Closer to interaction point
  → L0 radius from 24 mm to 19 mm
- Reduction of material budget per layer
  → from 0.36% X/X0 to 0.09% X/X0 (average)
- Homogeneous material distribution

ITS3 sensor bending

ALPIDE CHIP BENDING

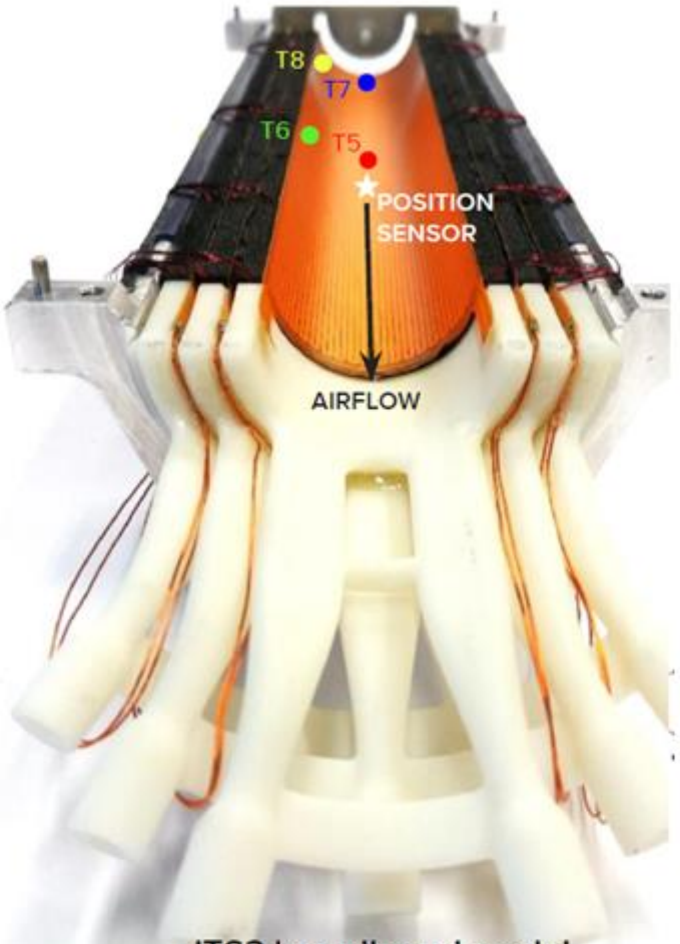
- Project target for thicknesses and bending radii are in a “not breaking” regime
- Full mock-up “µITS3”: 6 ALPIDEs (180nm) bent to ITS3 target
- No degradation of detection efficiency and spatial resolution observed
- Results validated on bent 65 nm pixel test structures





First results on bent MAPS:
G. Aglieri Rinella et al Nuclear Inst. and Methods in Physics Research, A 1028 (2022) 166280

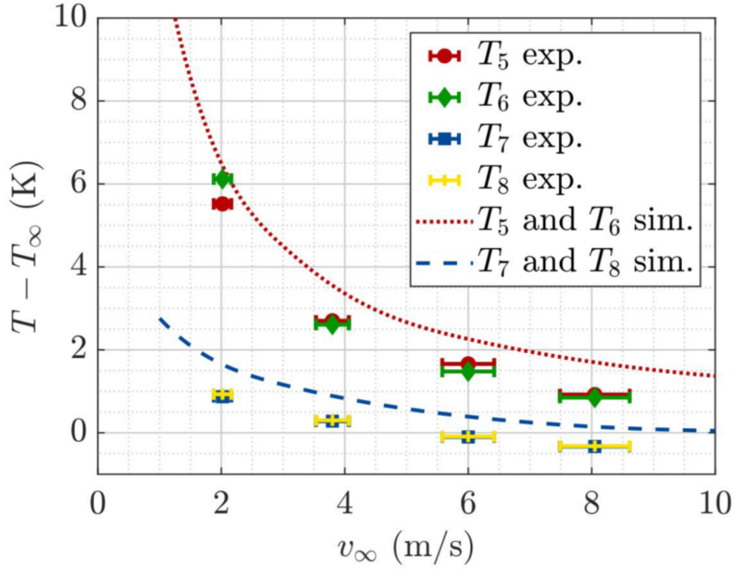
Air cooling - Thermo-mechanical characterization



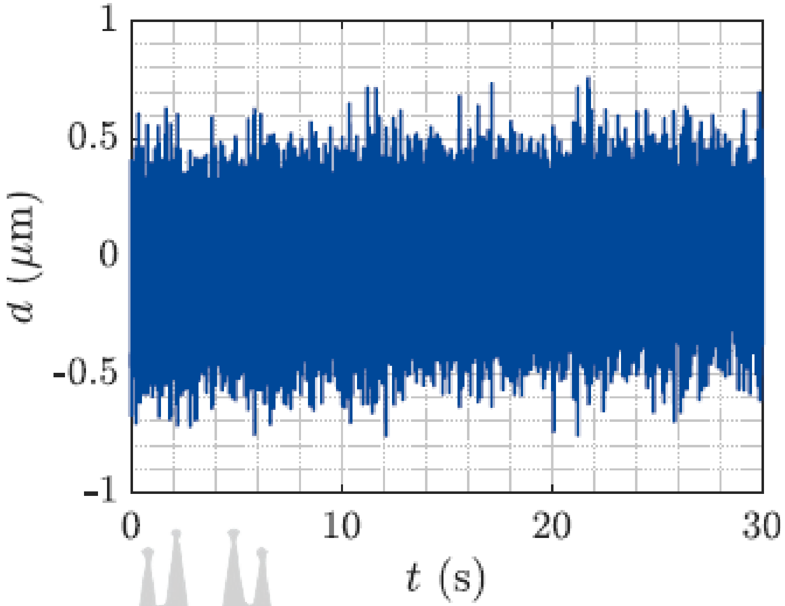
ITS3 breadboard model

Tests in wind tunnel on breadboard model:

- Si and polyimide sandwich with copper serpentines embedded
- exemplary power consumption: 1000 mW /cm^2 in end-caps, 25 mW /cm^2 in matrix
- $\Delta T < 5$°C and vibrations within ± 0.5 μm with 8 m/s airflow



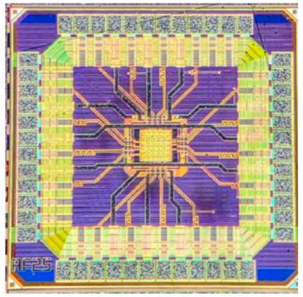
(c) Layer 0 - Matrix



MLR1: 65 nm technology qualification

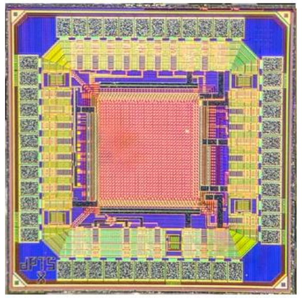
Main goals:
- Learn technology features
- Characterize charge collection
- Validate radiation hardness

MLR1 contains many test chips (transistor test structures, DACs, analog pixel matrices, digital pixel matrices, ...)



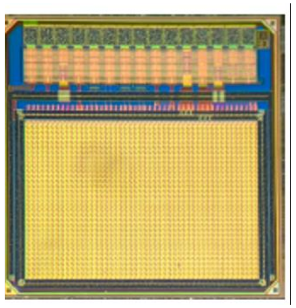
APTS

Analogue Pixel Test Structure
- 4x4 px matrix with direct analog readout
- OpAmp buffer for enhanced time resolution
- SF buffer for stable readout



DPTS

Digital Pixel Test Structure
- 32x32 px matrix with digital asynchronous readout

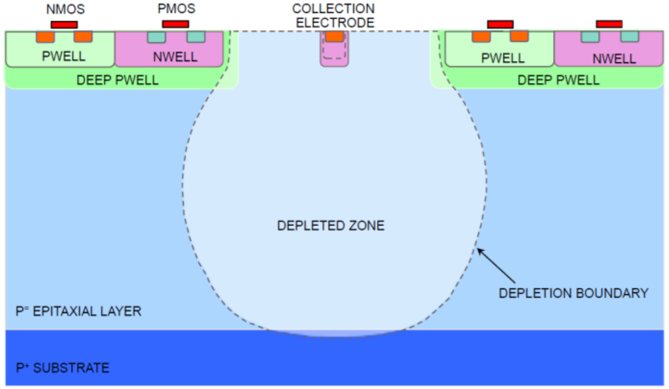


CE65

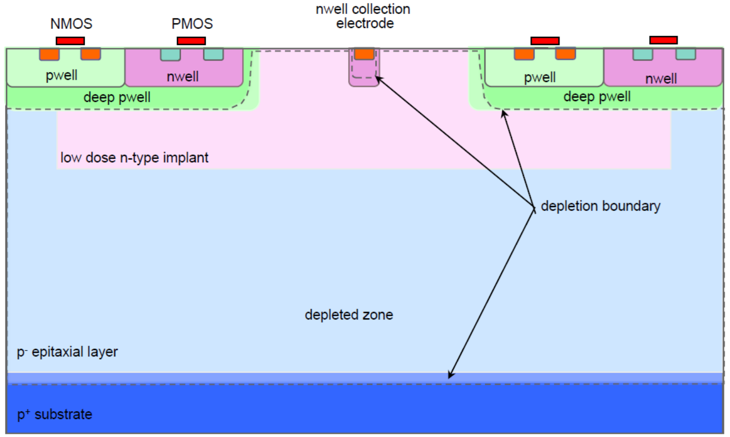
Circuit Exploratoire 65 nm
- 64x32 px matrix with rolling shutter analog readout

Process modification

Standard



Modified with gap



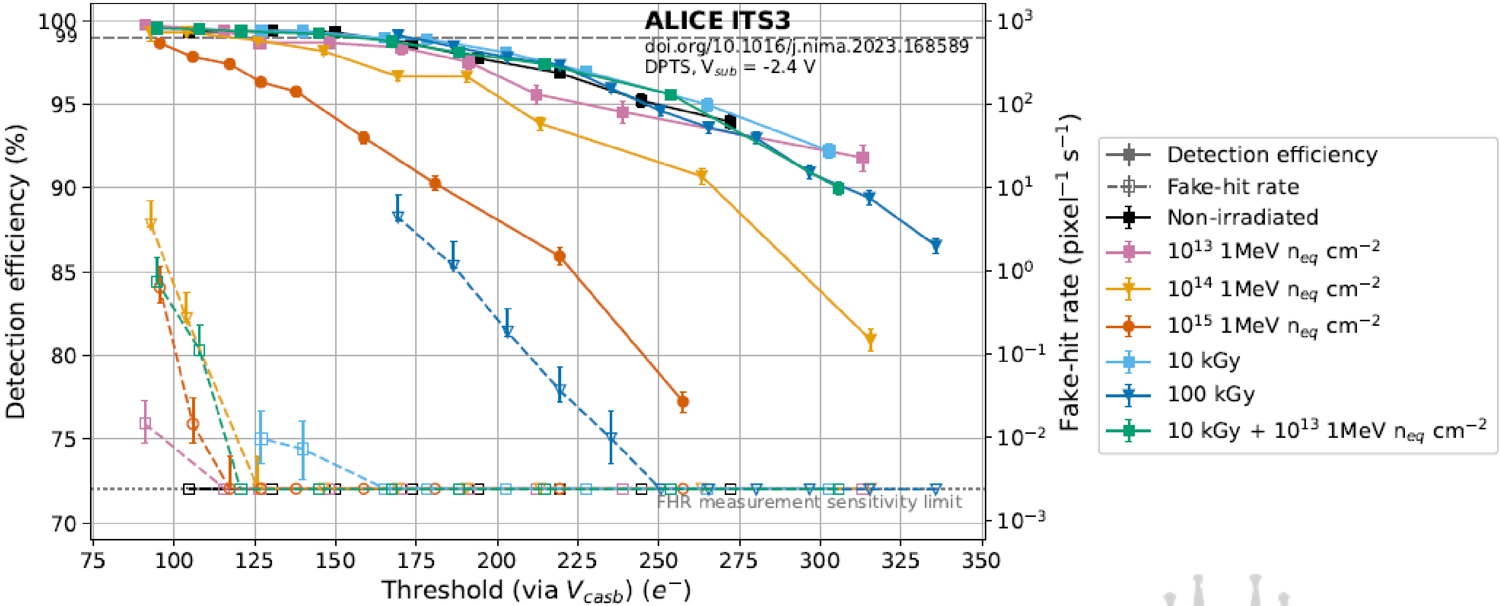
- Standard: ALPIDE-like
- No fully depleted → signal charge outside the depleted area collected primarily by diffusion
- Tolerance to NIEL exceeding 10^{13} 1 MeV neq/cm^2

- Most promising variant
- Gap in the deep n-implant to increase the lateral electric field at the pixel borders
- Higher detection efficiency and improved timing performance at the corners

Radiation hardness

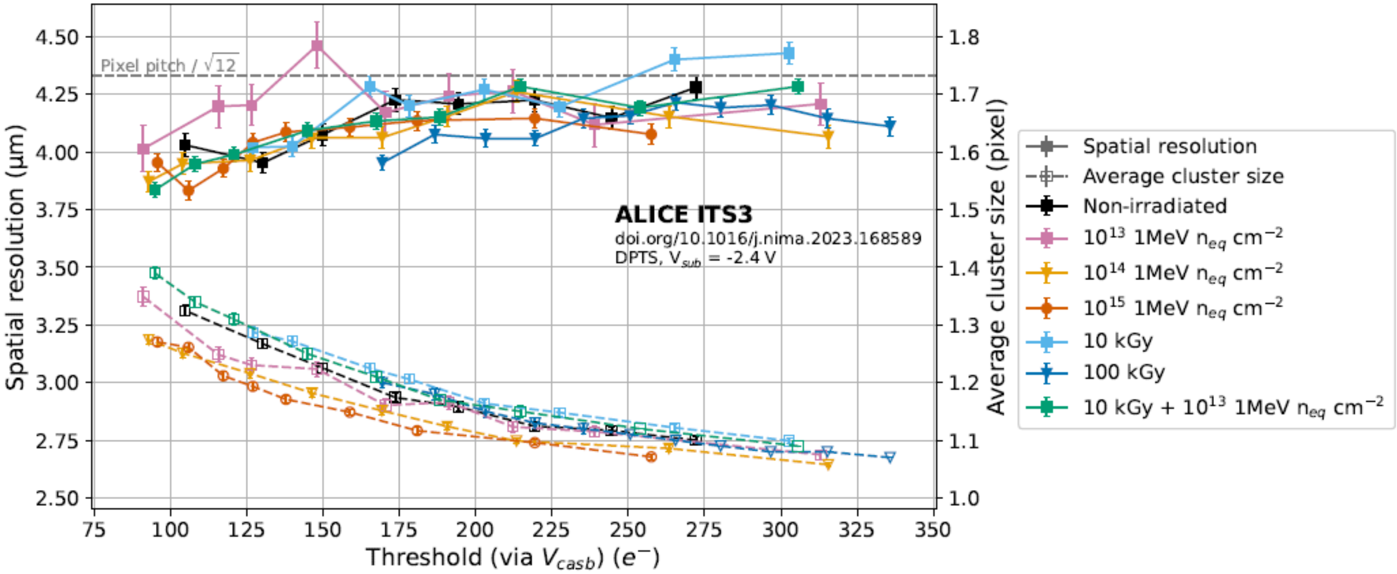
Detection efficiency and fake-hit rate Vs threshold and irradiation levels, as measured on 15 μm pitch DPTS:

- → Increased noise due to ionizing irradiation
- → Decreased CCE due to NIEL
- → Efficiency > 99% and FHR < 2 x10^{-3} pix^{-1}s^{-1} after irradiation at ITS3 requirements



DPTS: G. Aglieri Rinella et al Nuclear Inst. and Methods in Physics Research, A 1056 (2023) 168589
APTS: : G. Aglieri Rinella et al arXiv:2403.08952v1

Spatial resolution

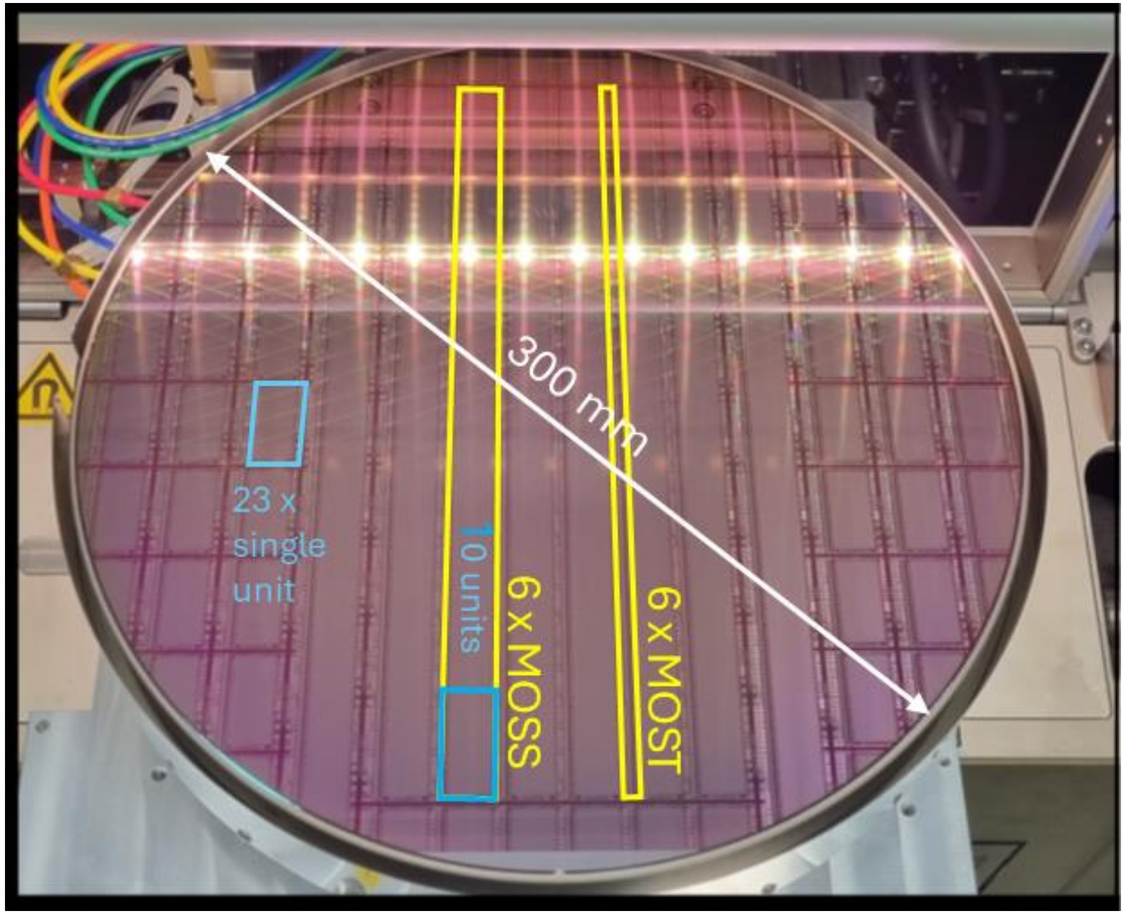


Spatial resolution and average cluster size Vs threshold and irradiation levels, as measured in testbeams on 15 μm pitch DPTS:

→ The spatial resolution measured slightly better than pixel pitch / √12 (no degradation with received dose)

→ Slight systematic decrease of average cluster size with the increasing non-ionising radiation dose

Stitched MAPS in Engineering Run 1 (ER1, 65 nm)



MOSS - MOnolithic **S**titched **S**ensor (14 x 259 mm^2)

- 6.72 Mpixel, different pitches (18 and 22.5 μm)
- Conservative design

MOST - Timing (2.5 x 259 mm^2)

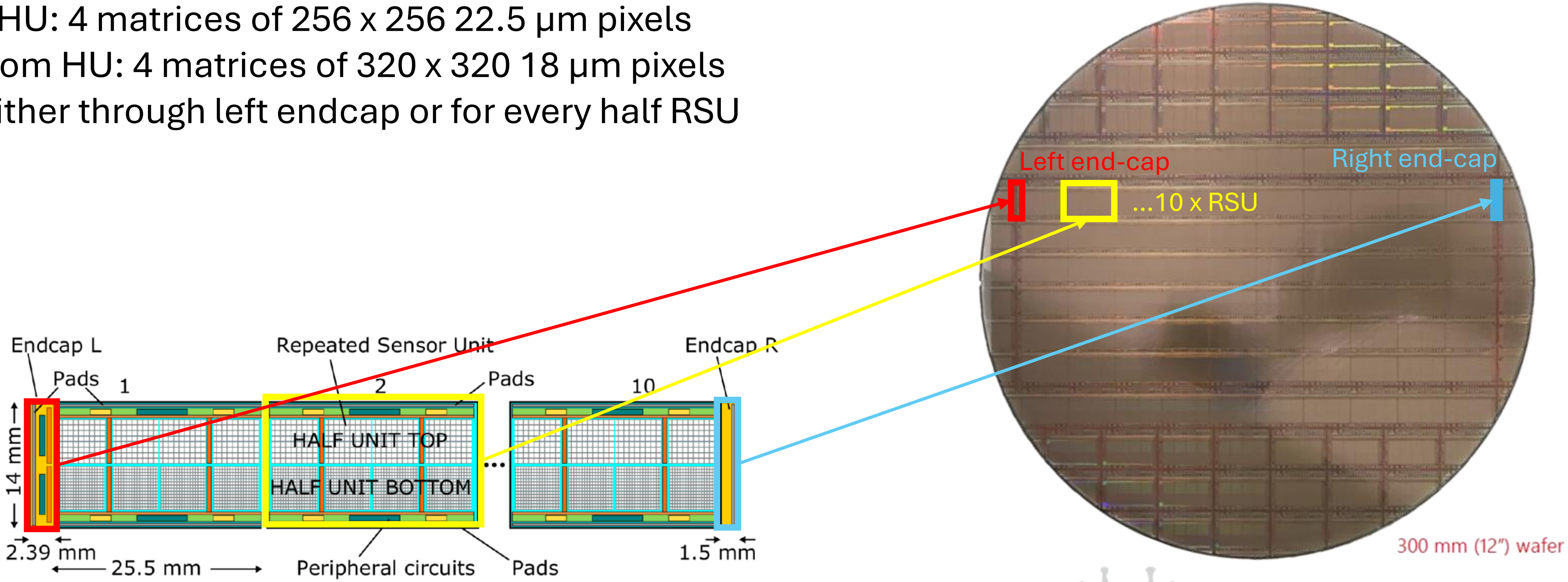
- 0.9 Mpixel , 18 μm pixels
- More dense design

Goals:

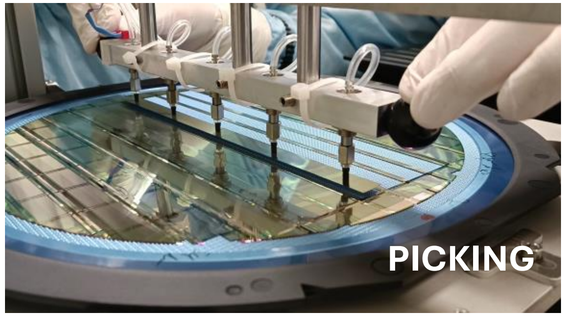
- Show feasibility of stitching process
- Understand stitching 'rules', redundancy, fault tolerance

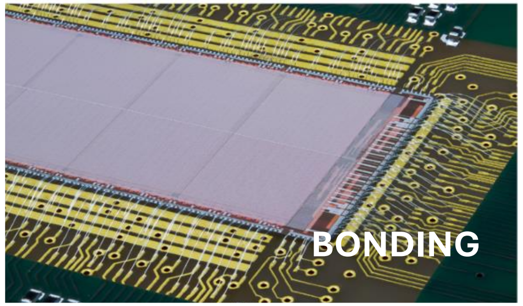
MOSS

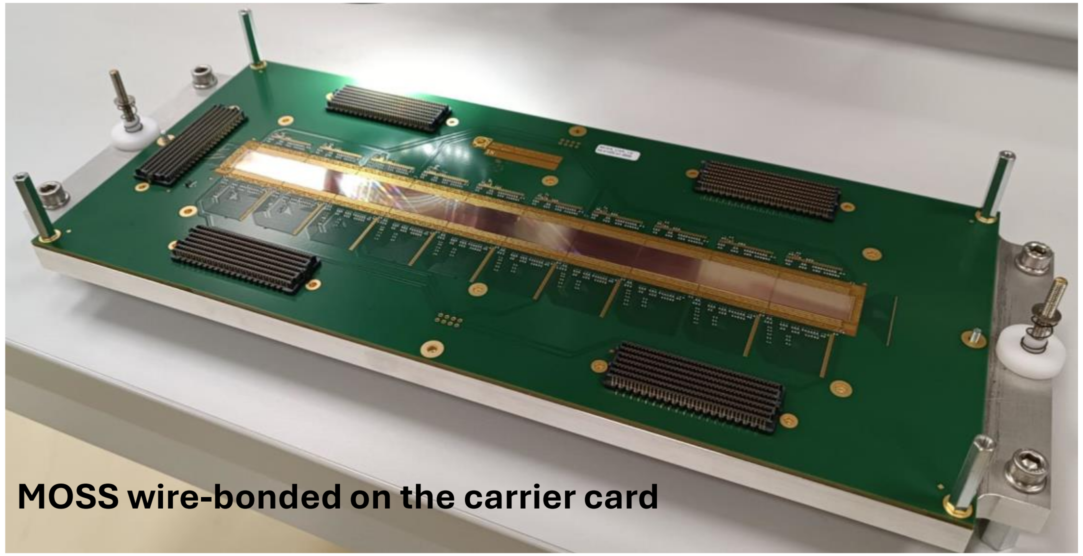
- 10 Repeated Sensor Units (RSU) & 2 end-caps regions (powering and readout)
- 2 independent Half Units (HU) per RSU
  - Top HU: 4 matrices of 256 x 256 22.5 μm pixels
  - Bottom HU: 4 matrices of 320 x 320 18 μm pixels
- Readout either through left endcap or for every half RSU separately

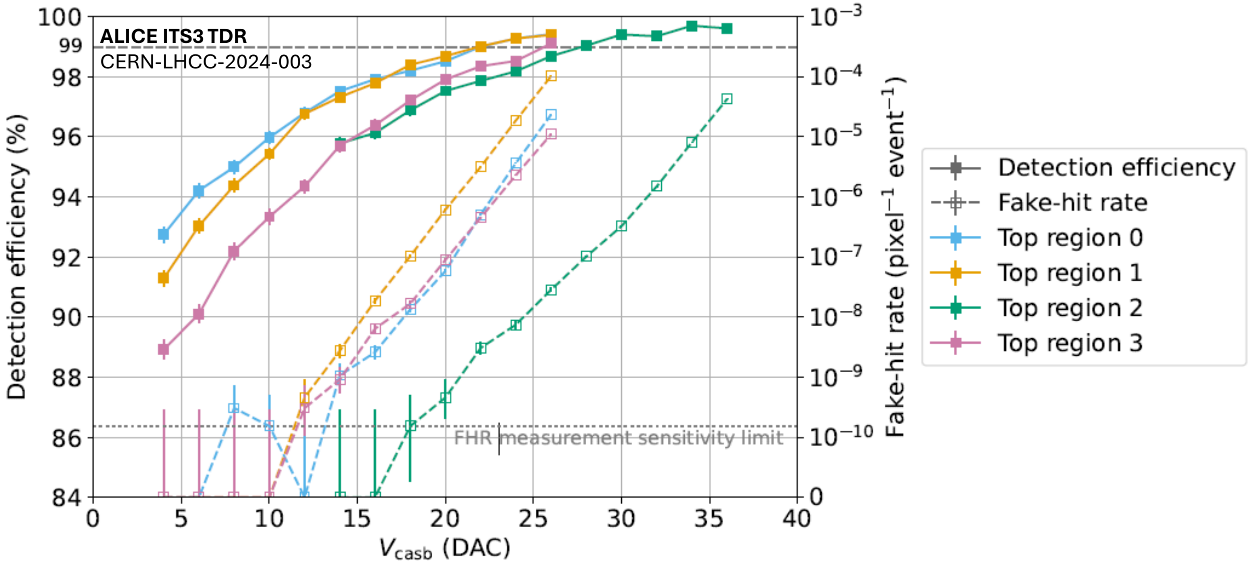


MOSS first testing results






MOSS wire-bonded on the carrier card

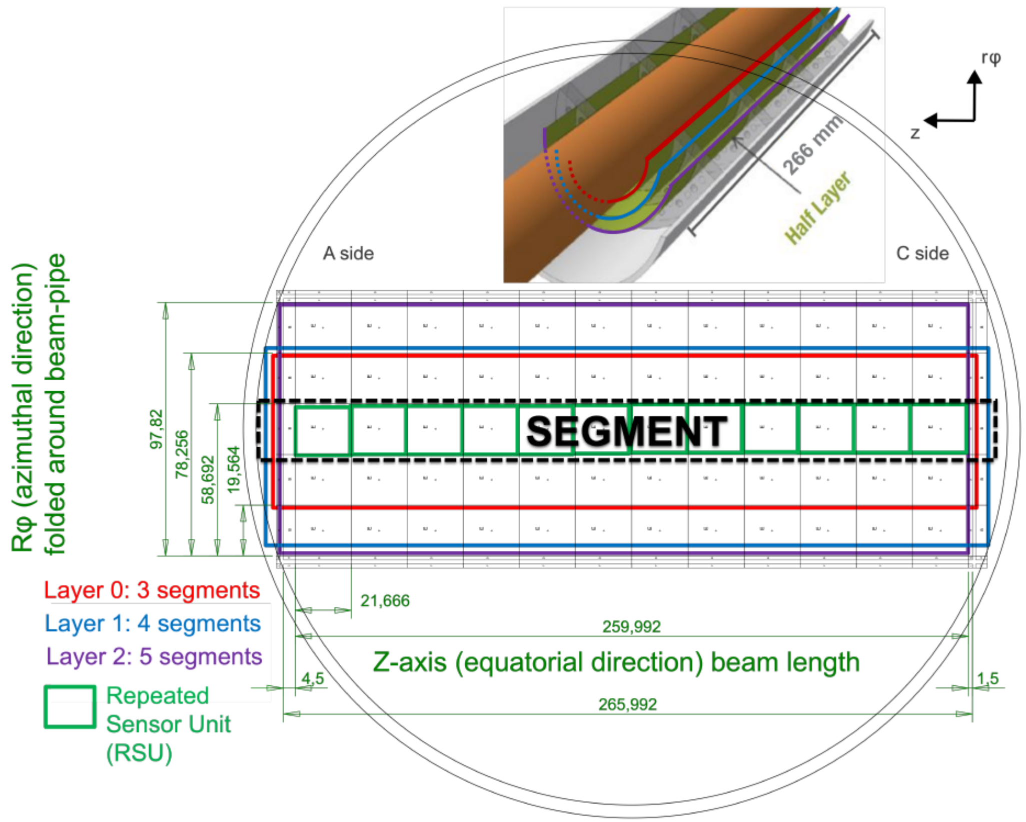


- Chip is operational
- Efficiency and spatial resolutions that are expected from MLR1 chips are confirmed
- Yield: currently under study with extensive characterization campaign with wafer prober. Target < 2% dead pixels per layer

Future ITS3 milestones

- **ER2 - full size prototype sensor**

Design according to final ITS3 specifications and finalised incorporating learnings from MLR1 and MOSS testing



- Modular design: each sensor is divided into 3, 4, or 5 segments with 12 RSUs
- Powering and readout only from end-caps
- End-caps acting as a separate readout circuit on the same silicon wafer
- Submission to the foundry in fall 2024

- **ER3 – final sensor production**

- **Optimization of assembly sequence and detector integration → qualification model (QM) half barrels**

- **Final assembly and commissioning**

Summary

Major milestones achieved:

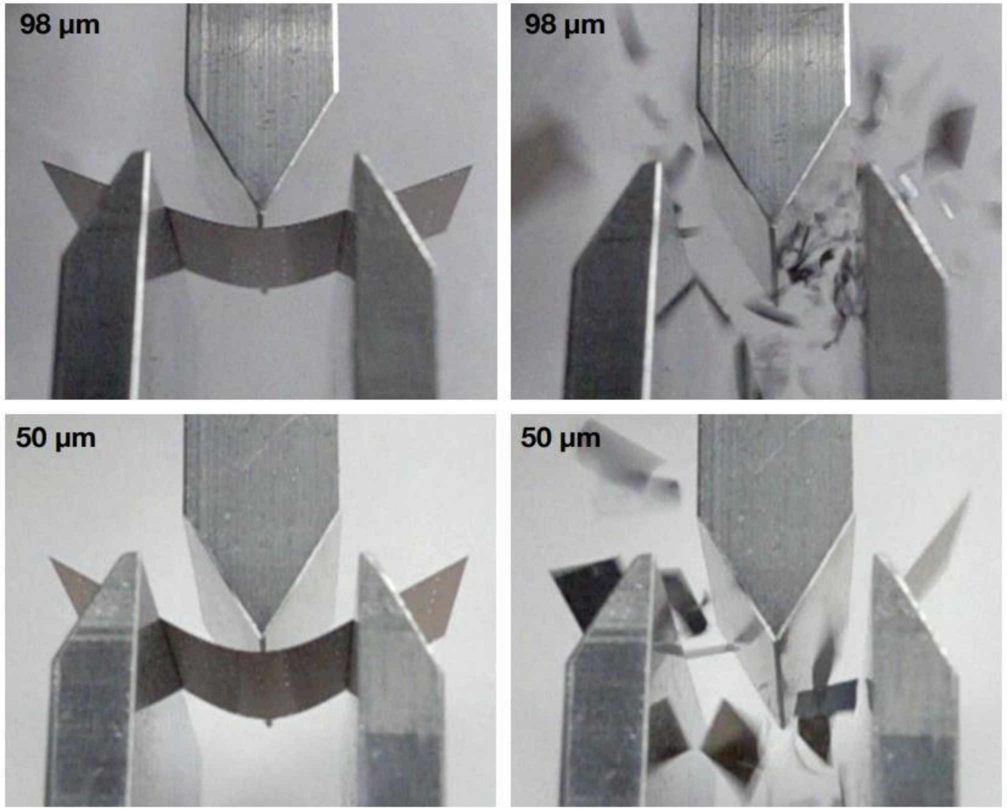
- Bending , interconnection , air cooling , assembly verified
- Bent MAPS performance demonstrated in beam
- 65nm process qualified (MLR1)
- Stitching successfully demonstrated in MOSS, testing ongoing
- TDR reviewed by LHCC and approved by Research Board

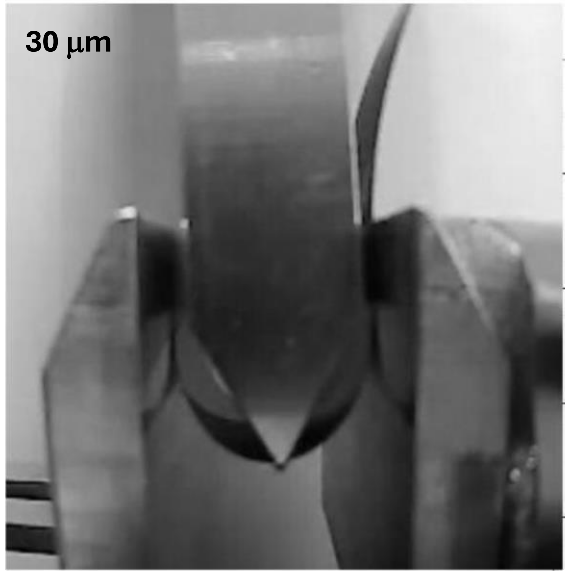
ALICE ITS3 is on track for installation in LS3 in 2026-2028!

Backup slides

ITS3 sensor bending

- MAPS of ~50 µm thickness are quite flexible
- The bending force scales with thickness to the third power → large benefit from going even a bit thinner
- The breaking point moves to smaller bending radii when going thinner

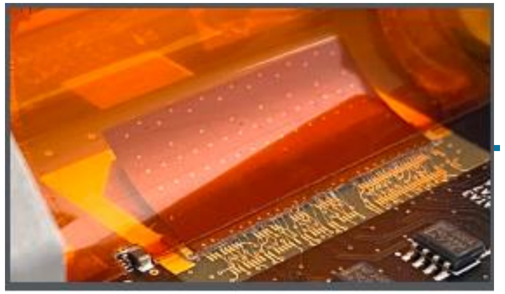




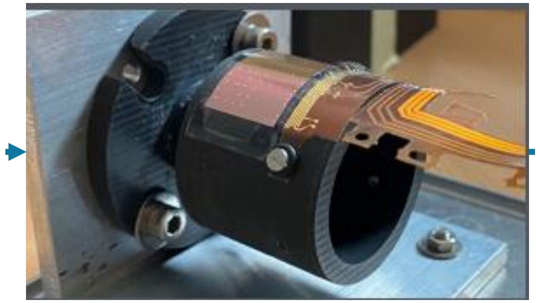
ITS3 sensor bending

Beam test campaigns on bent ALPIDEs:

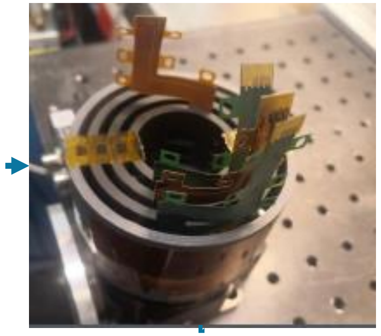
1. First bent chip (DESY, Jun 2020)



2. Bent chip on cylinder (DESY, Aug/Dec 2020)

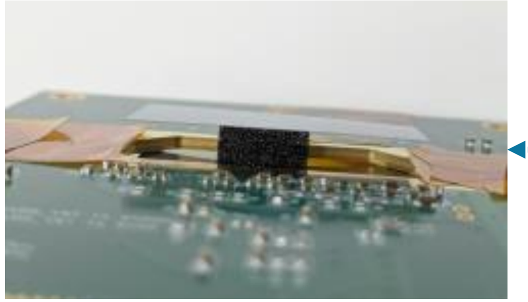


3. Bent chips at all radii, carbon foam (DESY, Apr 2021)

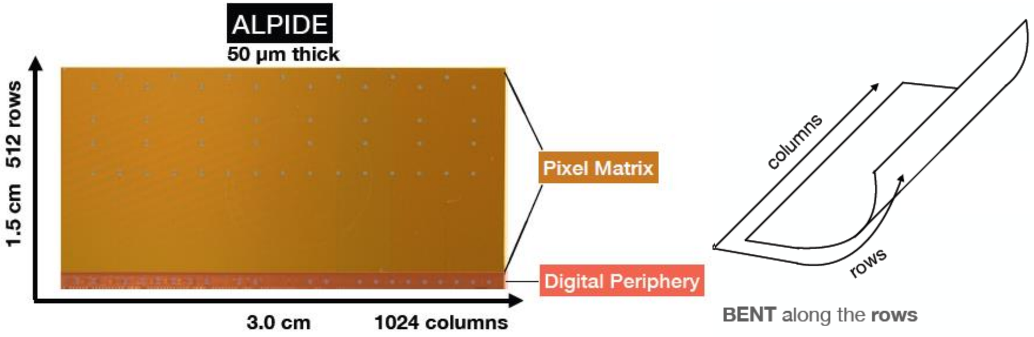


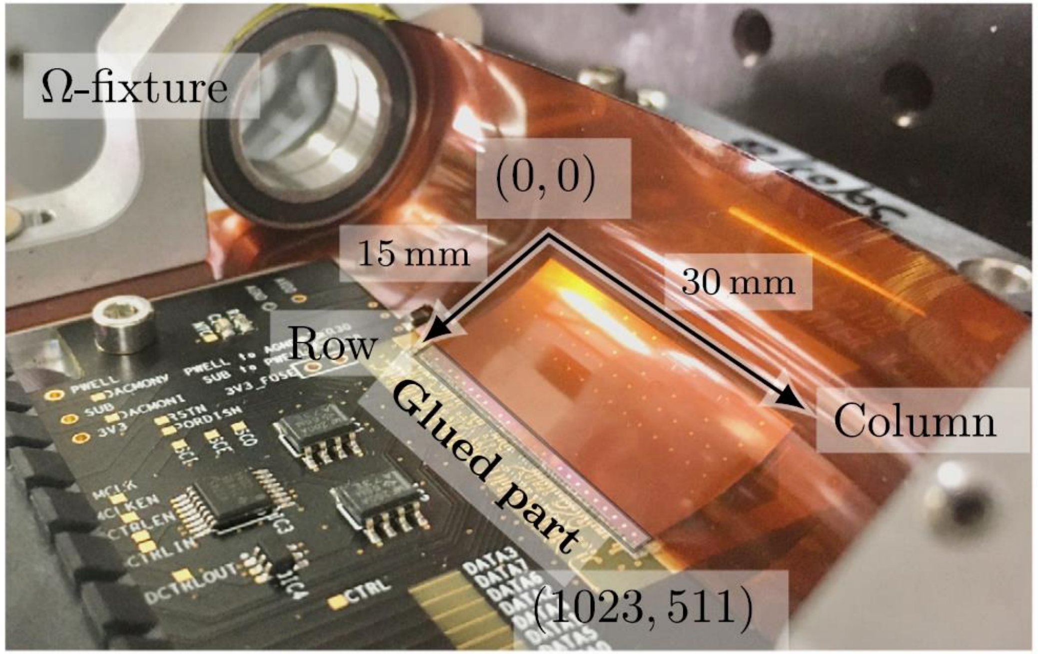
4. μITS3 with 6 ALPIDE + target (SPS, Jul 2021)

5. Carbon foam (DESY, Sep 2021)



ITS3 sensor bending

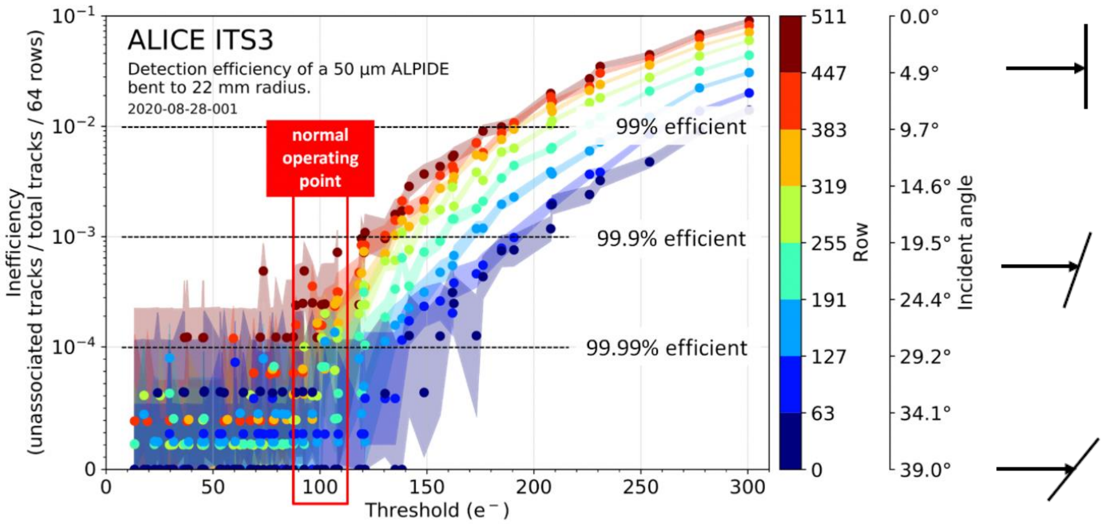




DESY, June 2020

Laboratory and test beam measurements

- Chip performance doesn't change after bending
- Efficiency above 99.9% at a threshold of 100 e- (normal operating point), consistent with flat ALPIDE

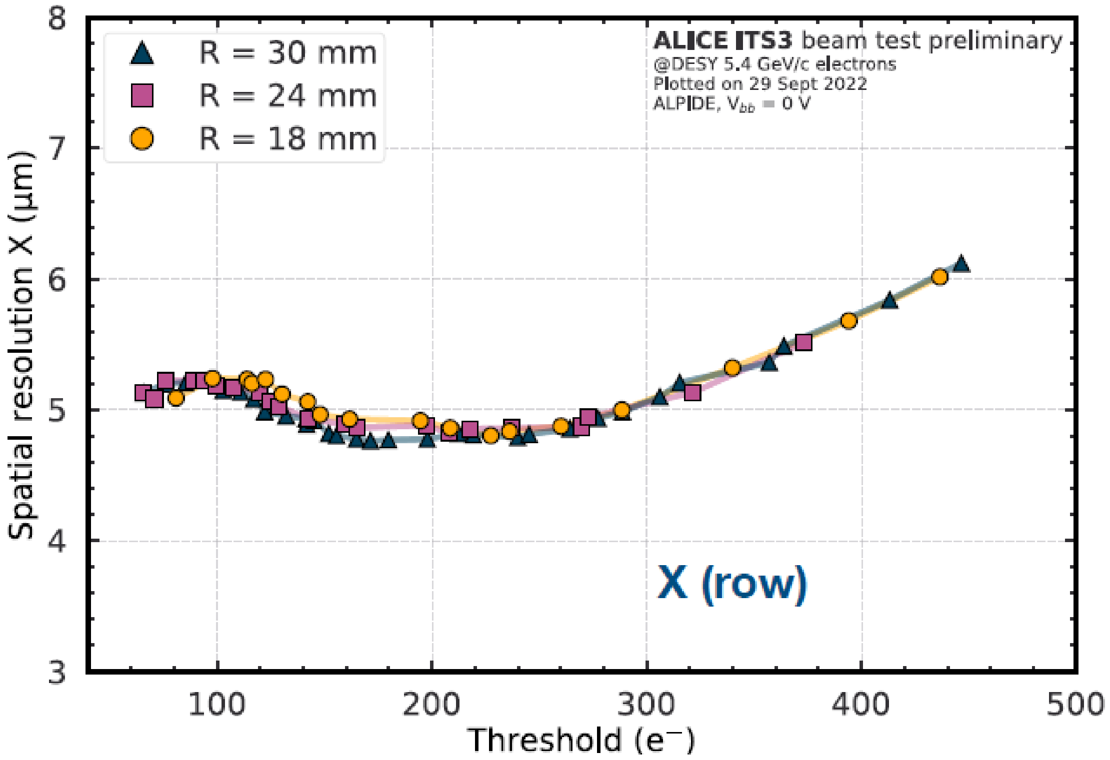


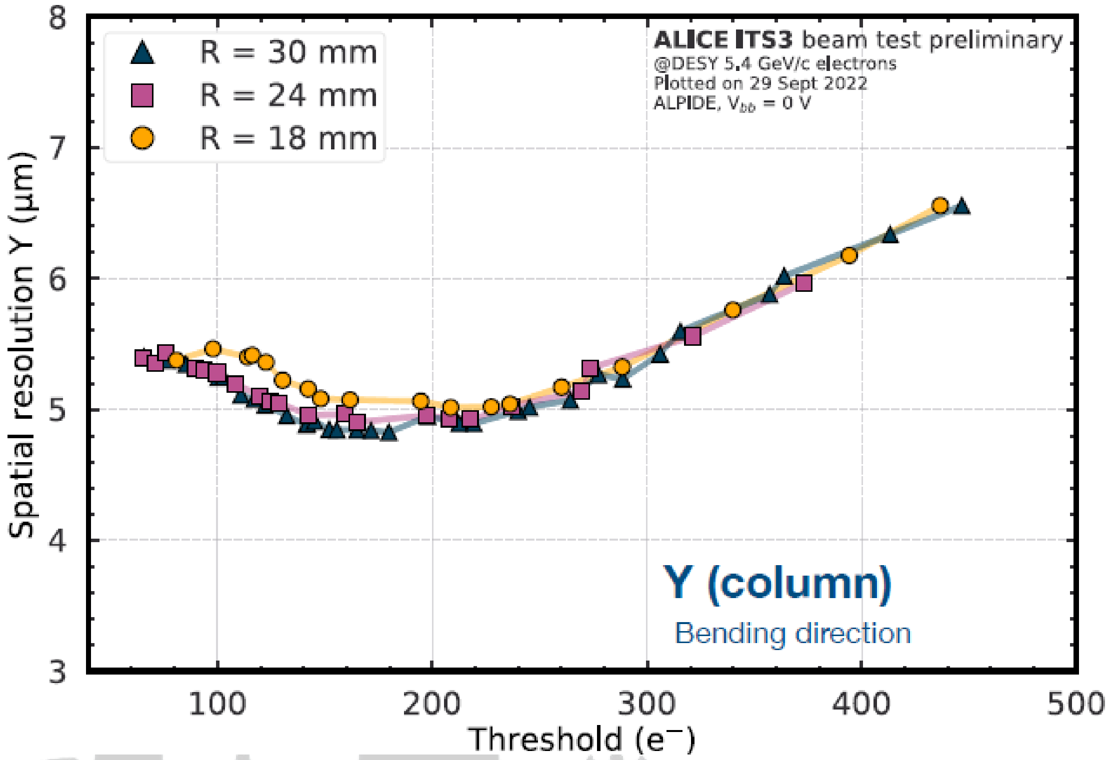
10.1016/j.nima.2021.166280

ITS3 sensor bending

DESY, Apr 2021

- No effects on bending radius observed
- Spatial resolution (~5 µm) and efficiency (> 99.99%) consistent with flat ALPIDE
- Results also match results where the chip was bent along the other direction





Measurement of Lamba-c (Λ_c)

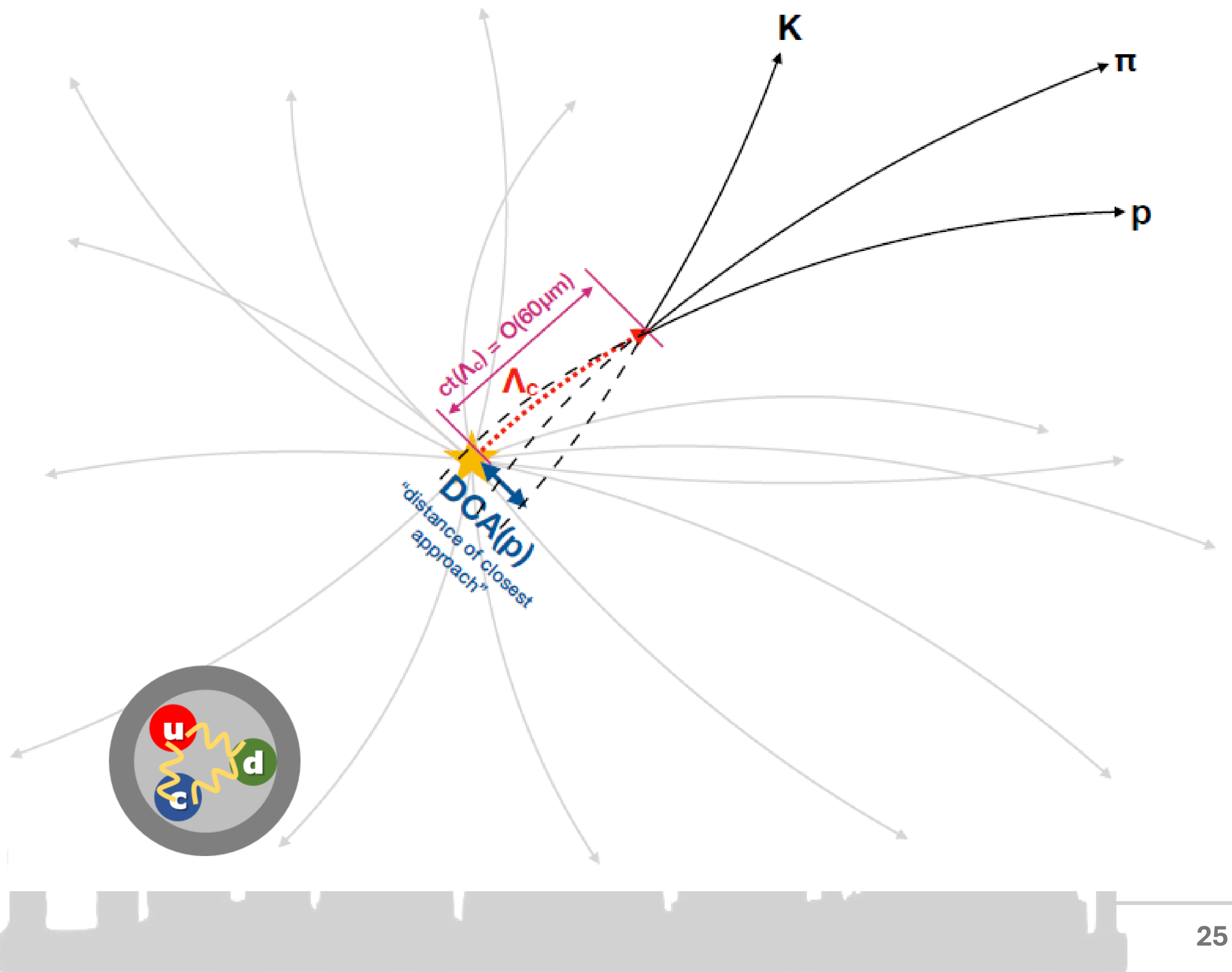
In heavy-ion collisions the production of charm and beauty baryons is expected to be significantly enhanced:

- recombination with light-flavour quarks present inside QGP
- hadron-mass-dependent radial collective flow

However current results have limited statistical precision!

The measurement requires very precise tracking and impact parameter resolution

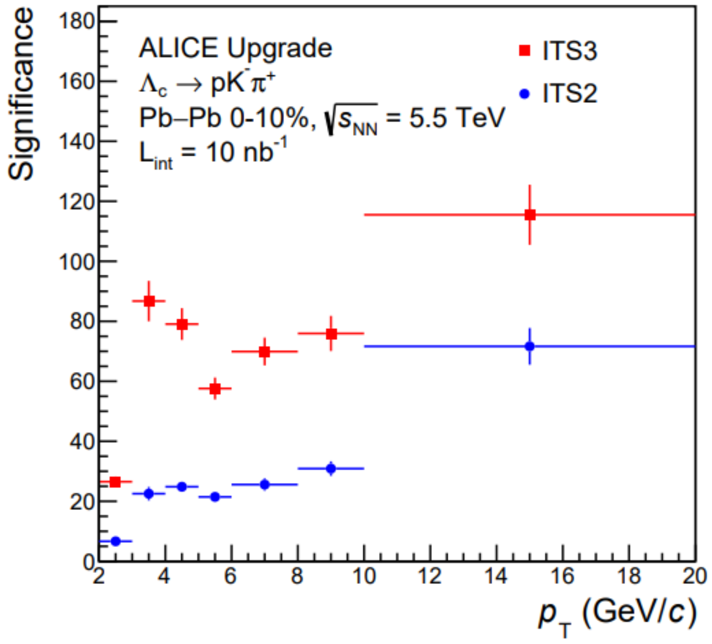
schematic view of a Λ_c decay

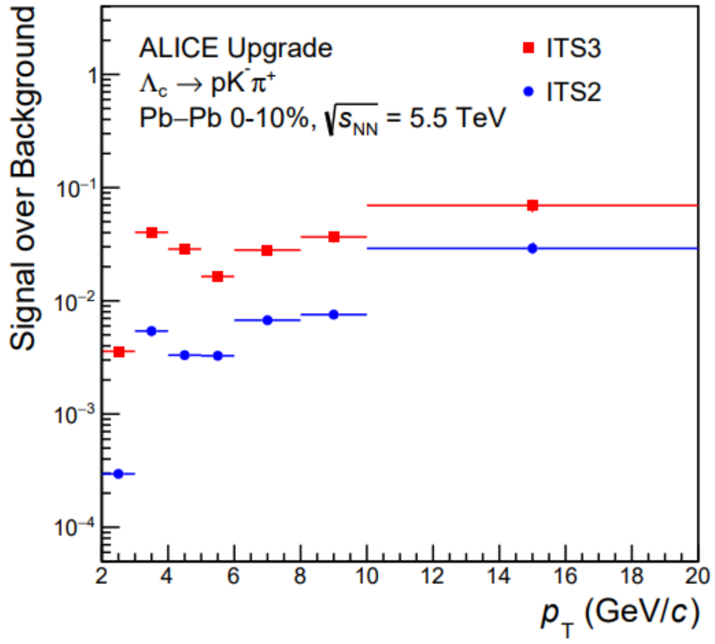


Measurement of Lamba-c (Λ_c)

Large improvement (wrt to ITS2) of significance (factor 4) and *S/B* ratio (10), thanks to:

- better pointing resolutions → larger rejection of the combinatorial background
- larger efficiency for the signal selection

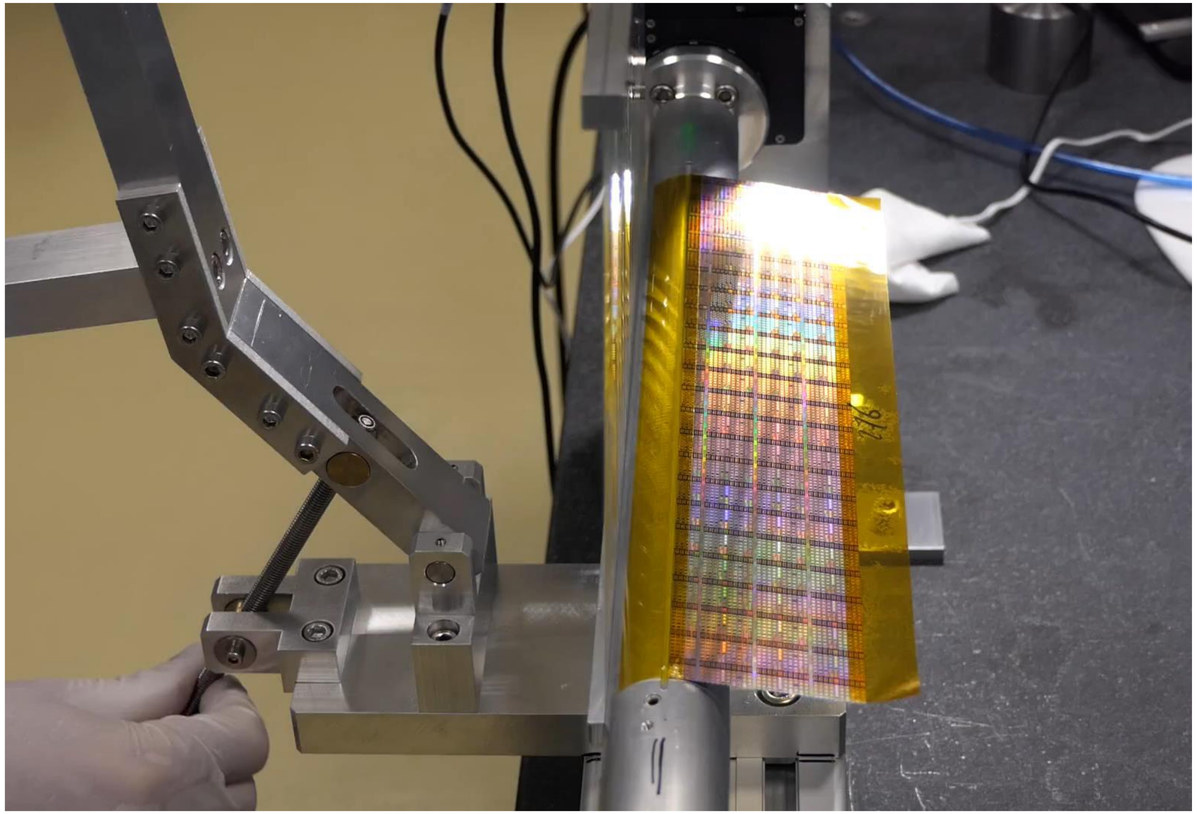


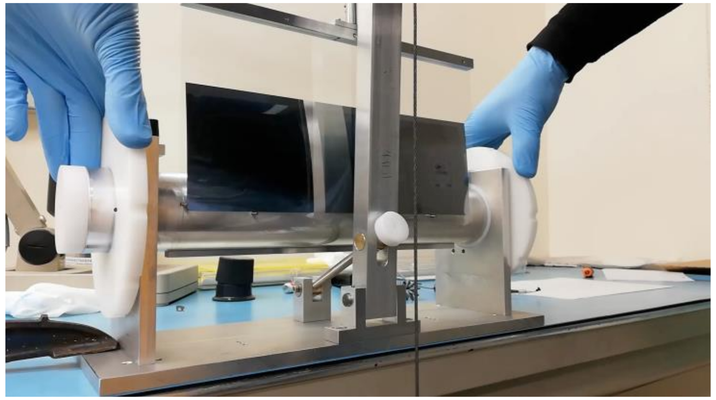


- Precise measurement of Λc/D ratio at low p_T
- Λc production → total cc cross section

BENCHMARK FOR ITS3

Bending Large Scale





Bending of a wafer scale sensor (50 µm thick, innermost ITS3 layer size)

Air cooling

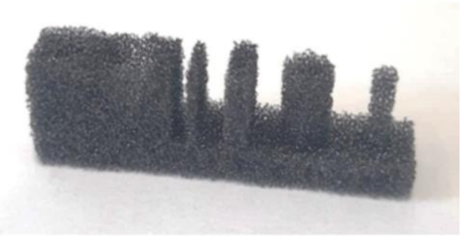
CARBON FOAM SUPPORT STRUCTURE

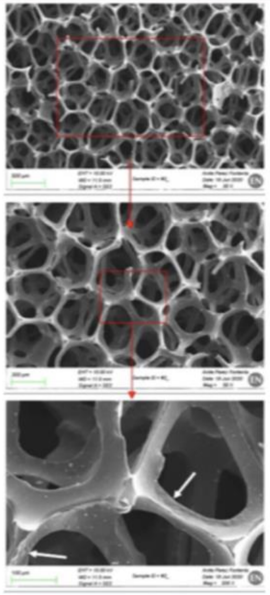
- Different foams were characterized for machinability and thermal properties
- Baseline is ERG DUOCEL_AR, which also features the largest radiation length

ERG DUOCEL_AR

0.06 kg/dm³

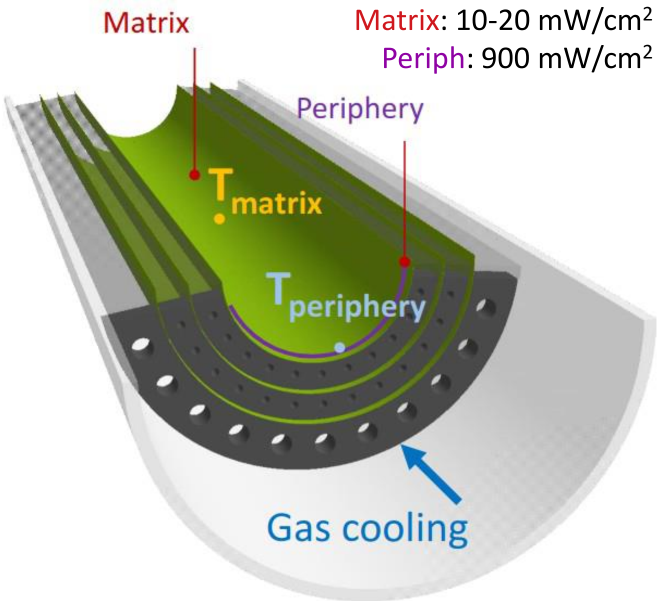
0.033 W/m·K



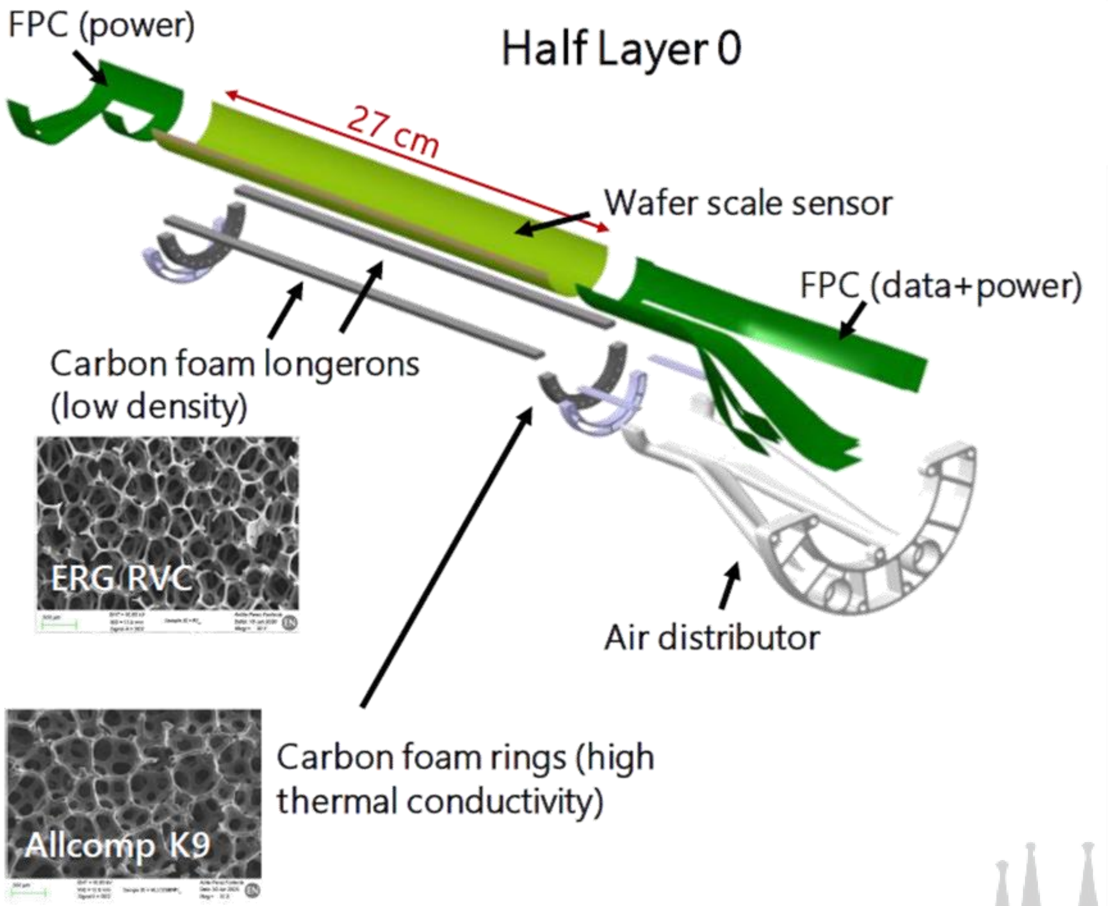


COOLING STUDIES: wind tunnel

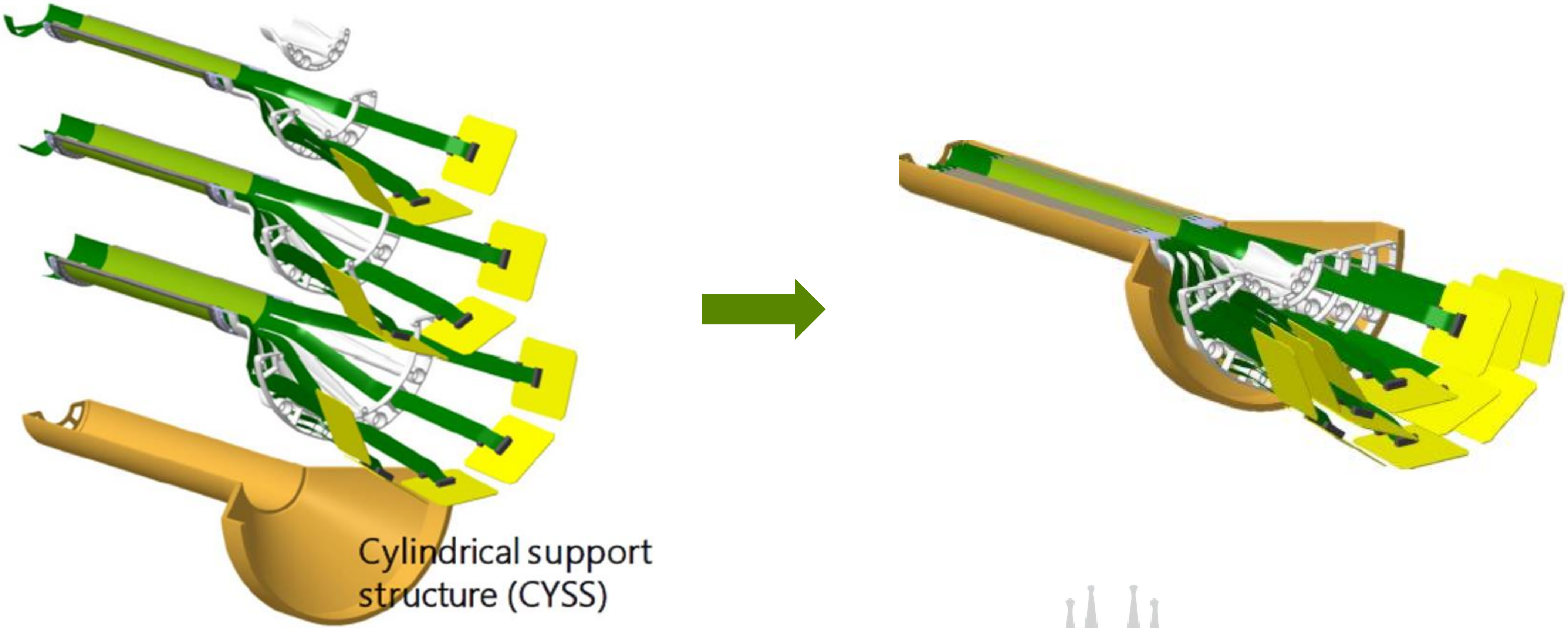
- Tests with model and heaters
- Different power & air speed (between 2 and 8 m/s)
- Thermal and mechanical properties are studied on estimated power consumption
- Carbon foam radiator are key for heat removal at periphery
- Air cooling is feasible with margin



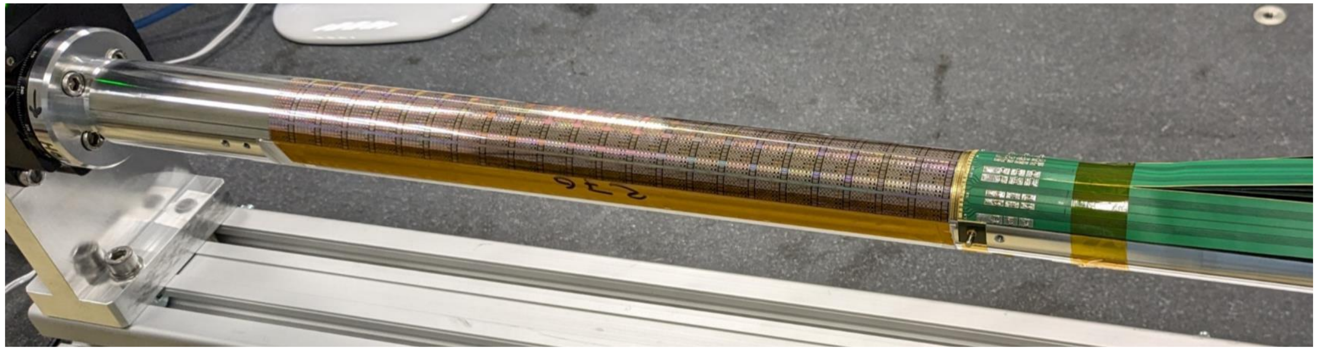
ITS3 Layout


FPC (power)
Half Layer 0
27 cm
Wafer scale sensor
FPC (data+power)
Carbon foam longerons (low density)
ERG RVC
Air distributor
Allcomp K9
Carbon foam rings (high thermal conductivity)

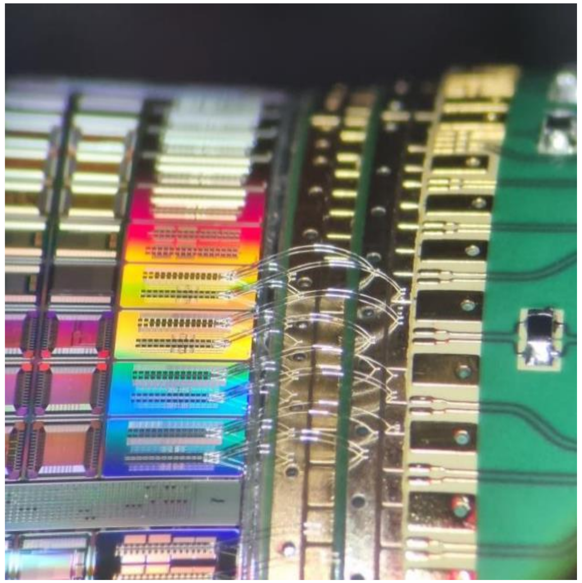
ITS3 Layout



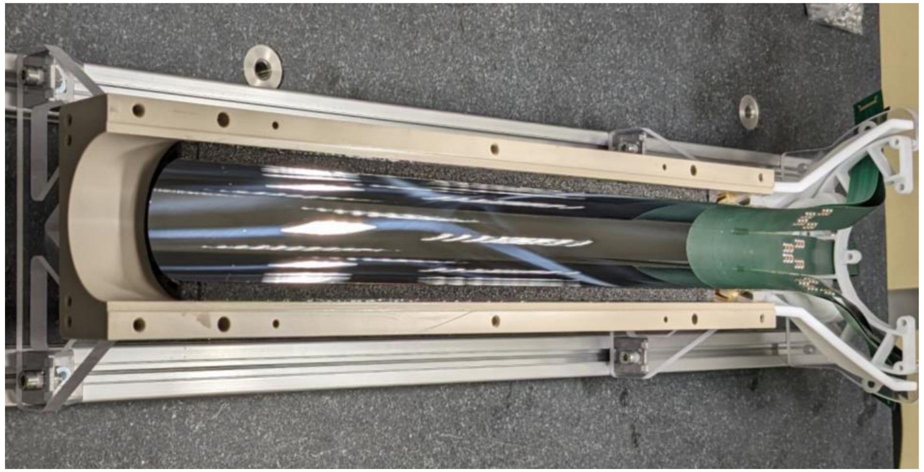
ITS3 assembly tests



FPC and Sensor on jig

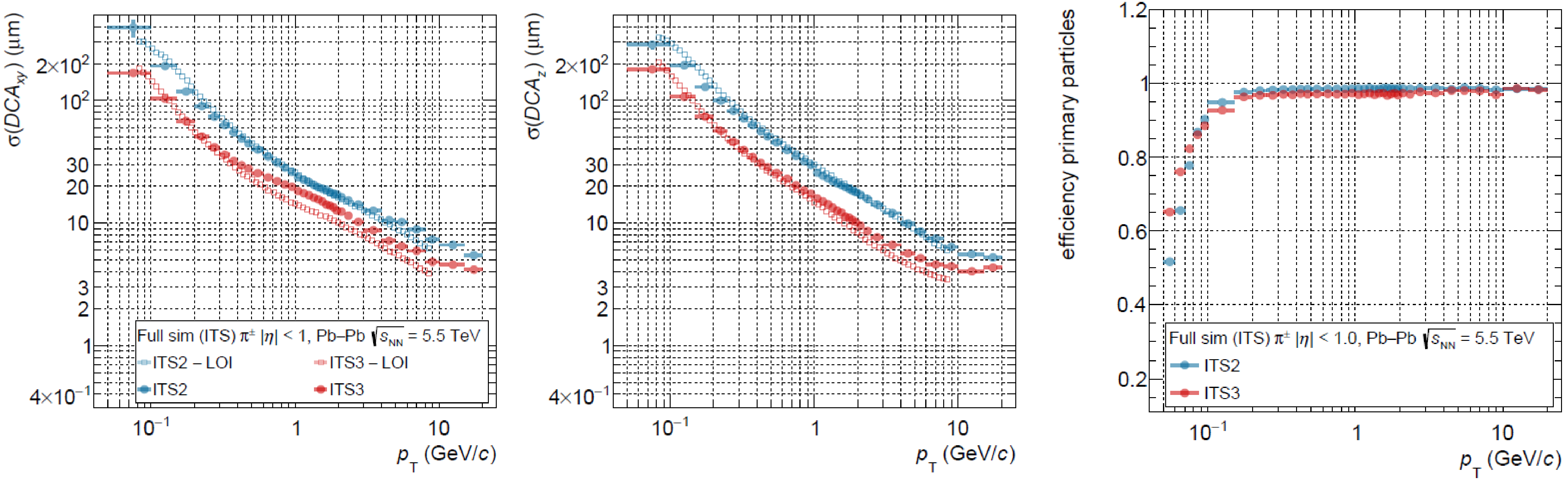


Wire bondings



First layer assembled

ITS3 Performance from simulations



Large improvement for low transverse momenta

Chip development roadmap

2021

MLR1: First 65nm process MAPS

2022

Successfully qualified the 65 nm process for ITS3

2023

ER1 - first stitched MAPS.
Two large stitched prototypes.
Goal: assess yield and stitching.
Tests ongoing.

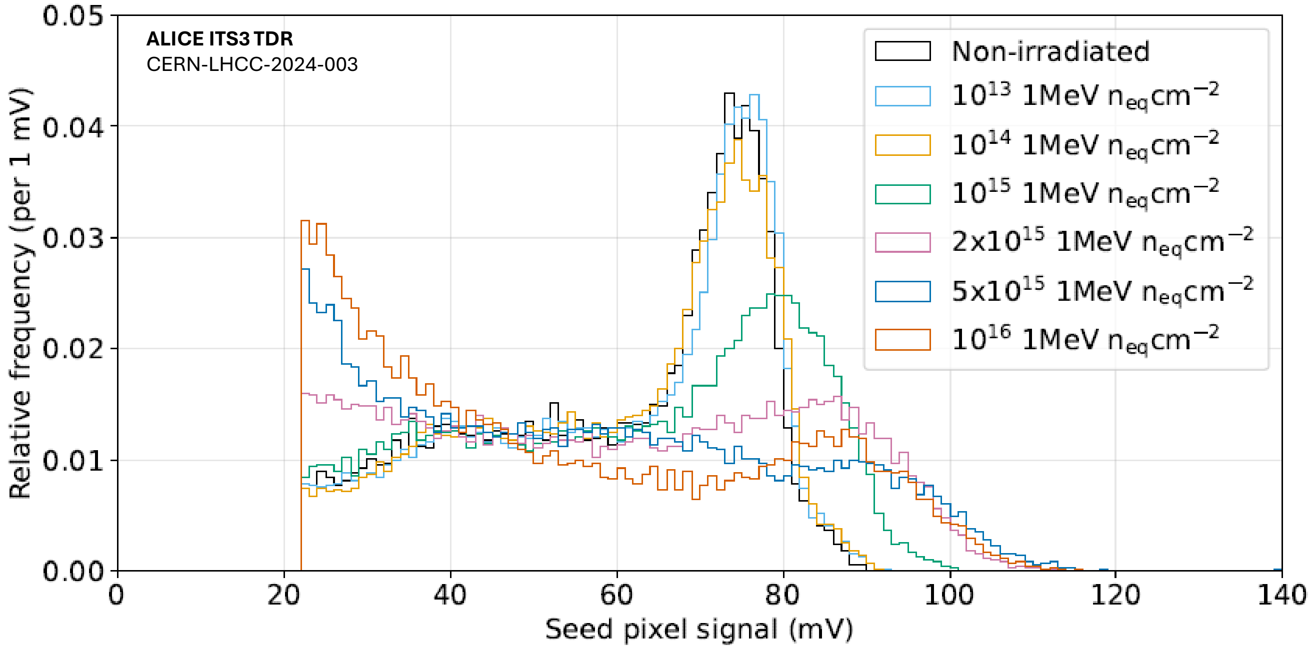
2024

ER2 - ITS3 sensor prototype.
Specifications frozen.
Design ongoing

2025

ER3 ITS3 sensor production

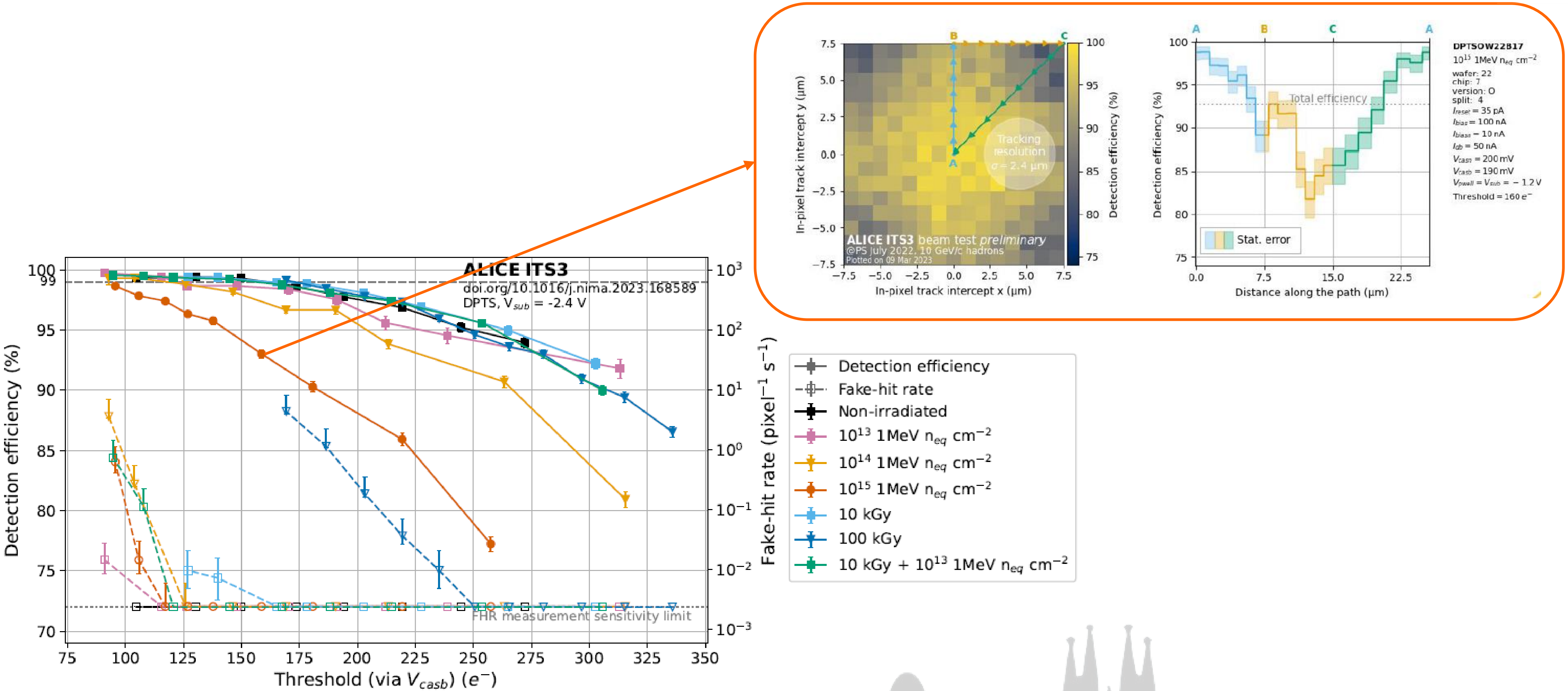
Radiation hardness



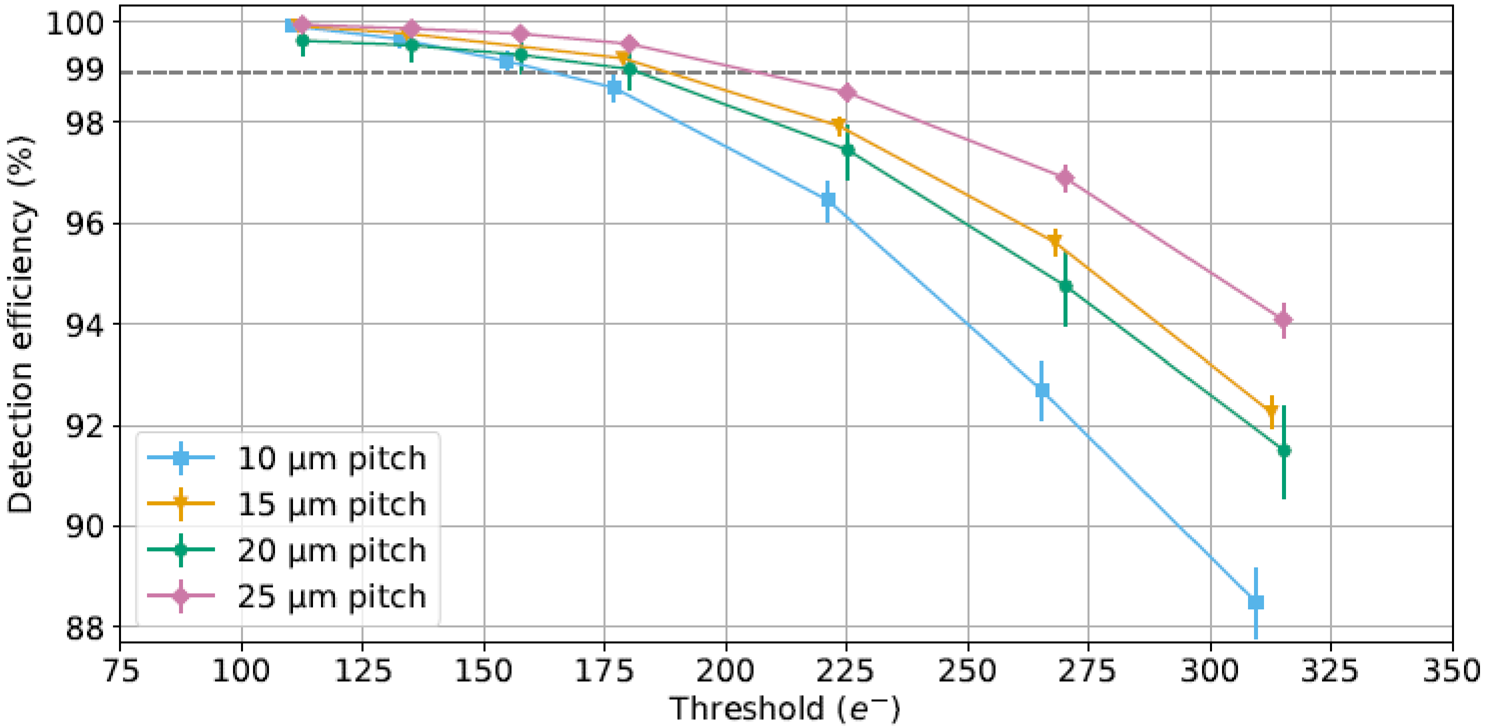
Seed pixel signal response to ^{55}Fe Vs irradiation levels, as measured on 15 μm pitch APTS:

→ Energy resolution degrades with the increasing non-ionising radiation dose

MLR1 - Radiation hardness



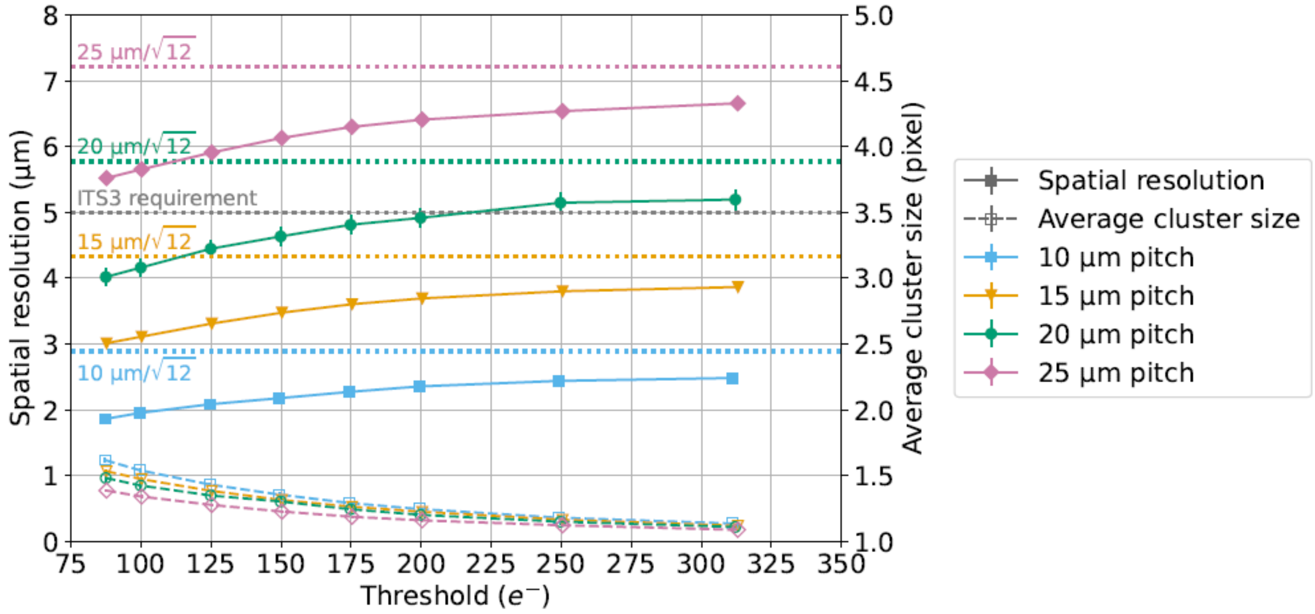
MLR1 characterization - pixel pitch

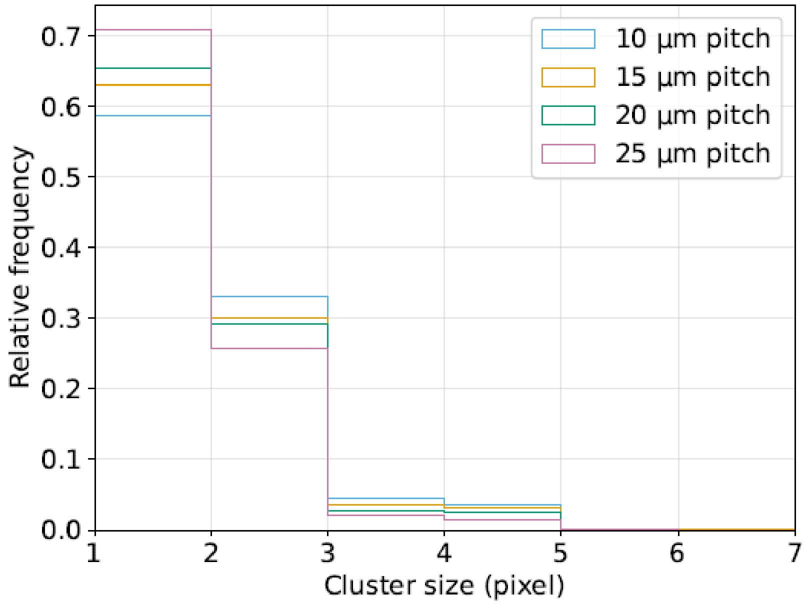


The detection efficiency increases with increasing pixel pitch

- Relative fraction of pixel border area decreasing with the increasing pixel pitch
- Pixel border only being less efficient due to geometrical sharing of the charge among neighbouring pixels

MLR1 characterization - pixel pitch

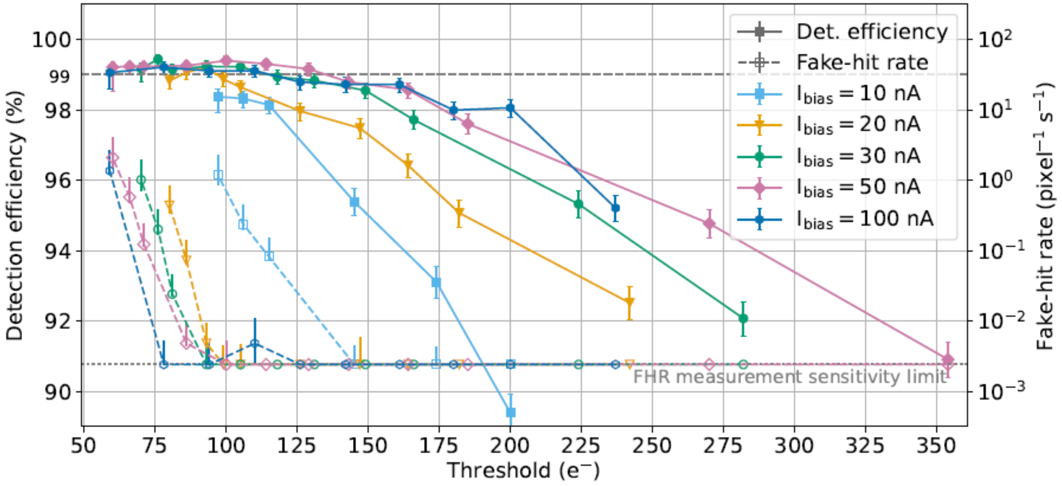




Spatial resolution and average cluster size VS threshold and pixel pitch, measured with APTS

- More charge sharing ⇨ improved resolution
- Considering the ITS3 target pitch size of 20.8 µm × 22.8 µm, the expected spatial resolution is about **5 µm** for a threshold of 100 e^-
- For the ITS3 it is expected to have on average less than **1.5 pixels** above threshold for a minimum ionising particle hit

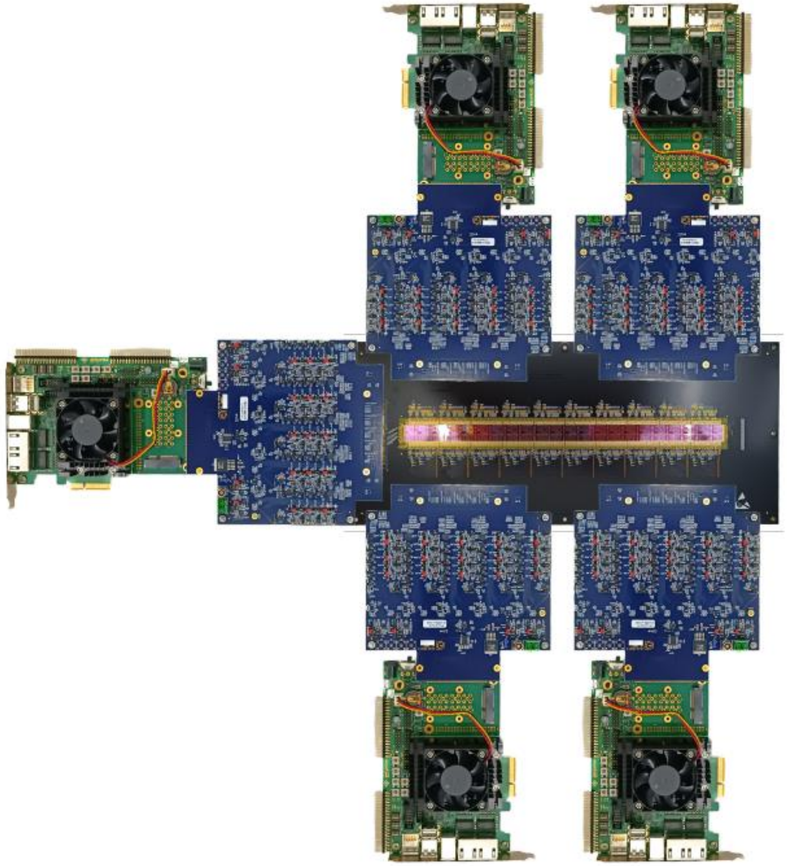
Power consumption

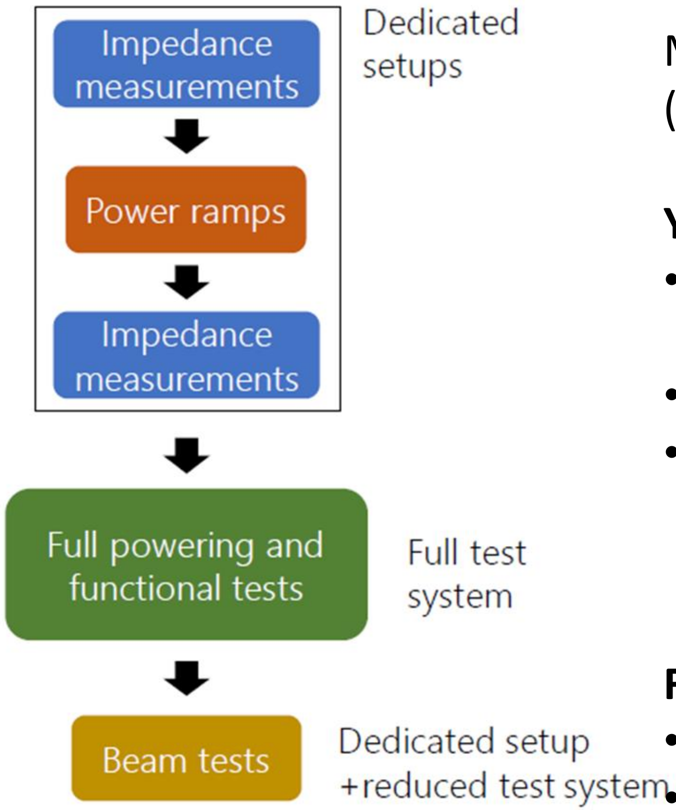


DPTS front end designed to investigate power consumption (ITS3 target < 40 mW/cm^2) :

- At least a main current I_{bias} of 30 nA is needed
- 16 mW/cm^2 as measured on 15 µm pixel
- 7.6 mW/cm^2 if projected to the final ITS3 sensor pixel pitch

MOSS tests





Impedance measurements

Power ramps

Impedance measurements

Dedicated setups

Full powering and functional tests

Full test system

Beam tests

Dedicated setup +reduced test system

MOSS chip from first production **97%** (97/100 chips) "OK"

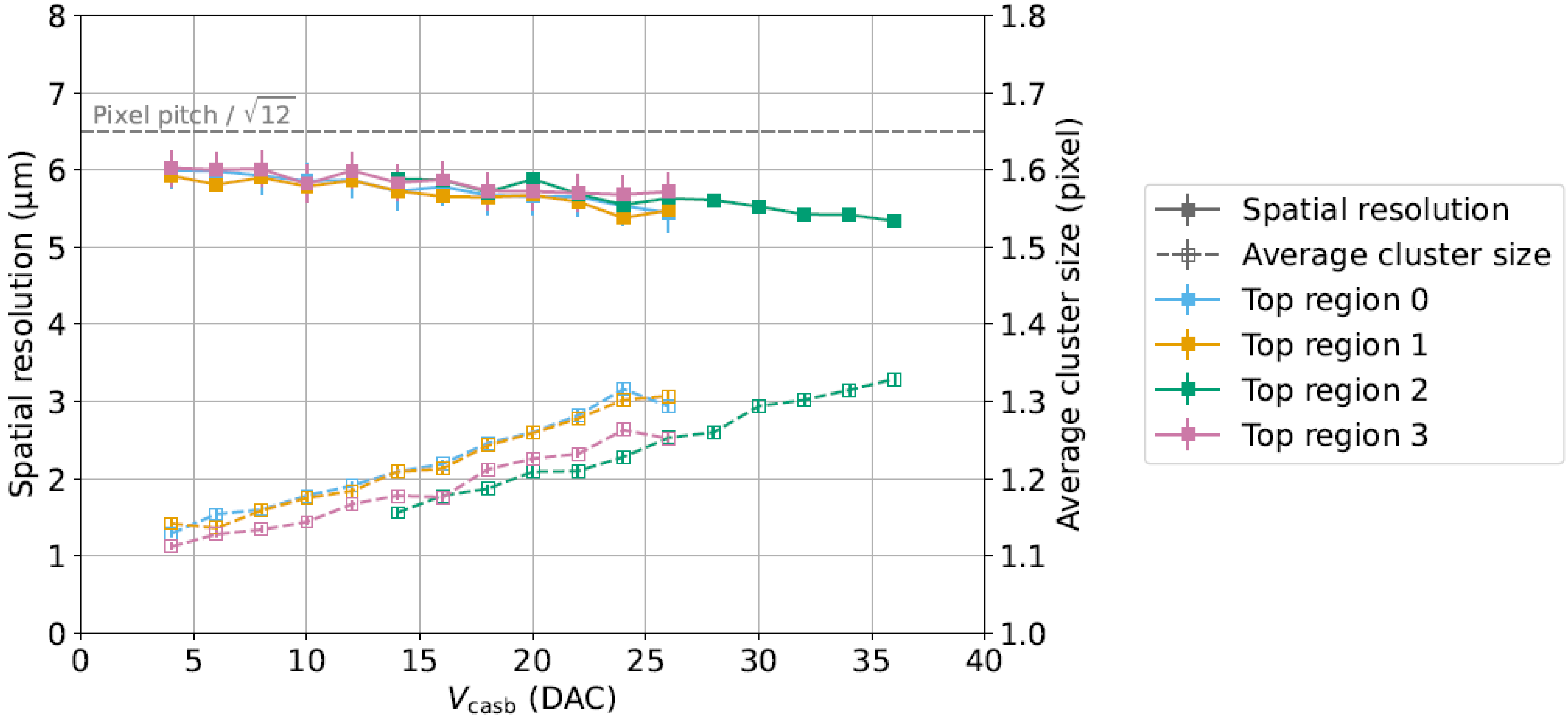
Yield:

- ≤ 2% missing pixels due to production yield
- 2/3 wafers comply
- 1440 regions (tiles)/sensor --> can be remotely switched off in case of production failure

Full ITS3 sensor production

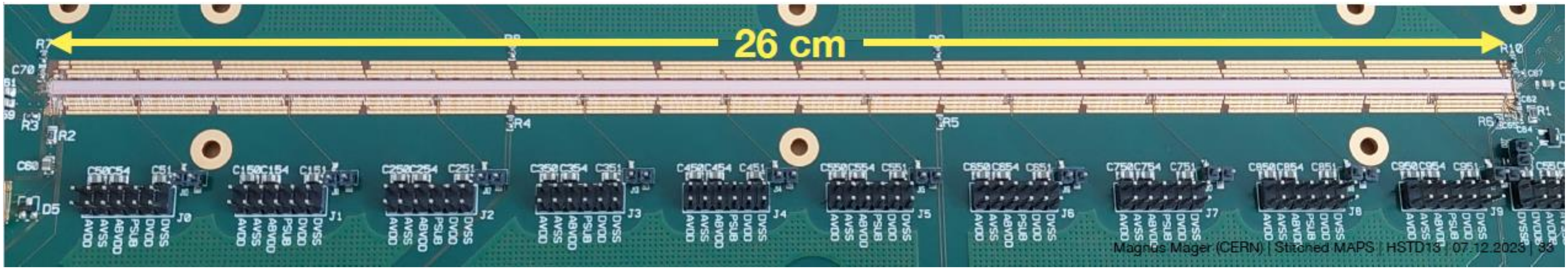
- 18 wafers from ER1 yield
- extrapolation plan to produce 50 wafers

MOSS tests - spatial resolution



MOST

- Power is distributed globally - yield is addressed by a highly granular set of switches that allow to turn off faulty parts locally
- Readout is purely asynchronous and hit-driven - low power consumption + timing information



Magnus Mager (CERN) | Stitched MAPS | HSTD13 | 07.12.2023 | 33

MOST - First communication tests

Serial transmission of hit data at bit rates of 1 Gbit s^{-1} over 26 cm-long columns

→ all 24 columns worked for the sensor tested, demonstrating robust cross-stitch signalling