### Energy ASIC for ECAL Upgrade II

### José Mazorra de Cos

#### Instituto de Física Corpuscular (CSIC-UV)



ECAL Upgrade II BCN-VLC - 3<sup>rd</sup> March 2023





#### • Simple OTA macromodel derived from Sedra & Smith 2009 Appendix B.1.1.







#### • Input capacitance and resistance, divided into differential and common.







#### • Independent common and differential gain.







#### • Compensated OTA, dominant pole through simple RC network.







#### • Model missing non-linear effects such as slew rate or saturation.







#### • NO output impedance, doubts in implementation for differential signal.







#### • Common testbench for DC, transient, AC and stability simulations.







#### • Output signal replicates input singal, but without saturating.





### OTA Testbench Transient



#### • Basic measurements implemented (overshoot, rise time, slew rate ...).

			Vsrc_cm	600 mV								
			Vsrc_diff	240 mV								
			Vin_cm	599.1 mV					Vop_trise	691.5 ps		
		i 📕 i -	Vout_cm	598.5 mV	s-vaa				Vop_tfall	691.5 ps		
			Vout_diff	240 mV		Vsp SR+	2.4 V/ns		Von_trise	691.5 ps		
			src+_high	720 mV		Vop SR+	-277.9 mV/ns		Von_tfall	691.5 ps		
			src+_low	480 mV	inp i	Vop SR-	277.6 mV/ns	115	Vo_trise	691.5 ps		
			srchigh	720 mV		Von SR+	-277.6 mV/ns		Vo_tfall	691.5 ps		
		d	srclow	480 mV	· · · i tinnin	Von SR-	277.9 mV/ns	<u>• • • • • • • • • • • • • • • • • • • </u>	Vop_tset1%+	1.483 ns	CØ	
		"	src_high	240 mV		Vo SR+	-555.8 mV/ns	diffstbprob	Vop_tset1%-	1.583 ns	ia 🕂 a-cia .	
		: : <b>†</b> 4	src_low	-240 mV		Vo SR-	555.2 mV/ns	•—n:2• 🌔 🔶	Von_tset1%+	1.483 ns	-	
		νυ(‡)	out+_high	718.5 mV	inn	Vop_OvrSht+	4.639 m%		Von_tset1%-	1.583 ns		
			out+_low	478.5 mV		Vop_UndrSht-	4.639 m%		Vo_tset1%+	1.483 ns	and	
		· · L	outhigh	718.5 mV		Von_OvrSht+	4.639 m%		Vo_tset1%-	1.583 ns		
			outlow	478.5 mV		Von_UndrSht-	4.639 m%		Vop_tset0.1%+	2.132 ns		
			out_high	240 mV		Vo_OvrSht+	4.639 m%		Vop_tset0.1%-	2.232 ns		
			out_low	-240 mV		Vo_UndrSht-	4.639 m%		Von_tset0.1%+	2.132 ns		
			out+_max	718.5 mV	·   · <u>*</u> ,	OvrSht_chck	4.639 m%		Von_tset0.1%-	2.232 ns		
			out+_min	478.5 mV		χvν -			Vo_tset0.1%+	2.132 ns		
			outmax	718.5 mV	2	1			Vo_tset0.1%-	2.232 ns		
			outmin	478.5 mV	<b>_</b> ^	W~ <b>-</b>			· · · ·			
			out_max	240 mV								
			out_min	-240 mV		Dere	Dth					
						RSIC	=кір					





• With  $R_{in}=1M\Omega$ ;  $C_{in}=10fF$ ;  $A_{0diff}=100k$ ;  $A_{0cm}=1$ ;  $R_{bw}=1k\Omega$ ;  $C_{bw}=16nF$ ;







• With  $R_{in}=1M\Omega$ ;  $C_{in}=10fF$ ;  $A_{0diff}=100k$ ;  $A_{0cm}=1$ ;  $R_{bw}=1k\Omega$ ;  $C_{bw}=16nF$ ;













# PZ Cancellation Shaper



#### • OTA macromodel based shaper design still with ideal components.





# PZ Cancellation Shaper



#### • Testbench with parametric FLW source to select pulse shape.





# PZ Cancellation Shaper Poly



#### • Polystyrene shape almost fits clock period, but weird tail effect.





# PZ Cancellation Shaper GFAG



#### • GFAG shape not fully available, but shaper reaches 25ns.







#### • OTA macromodel based integrator design still with ideal components.







• Testbench with constant voltage and parametric gaussian pulse options.















#### • Unity gain fitted for $\sigma$ =10ns gaussian centered in clock cycle.







### Track & Hold



#### • OTA macromodel based T&H design with bottom plate disconnection.







• Testbench with constant voltage and voltage ramp options.









• Clock generation follows ICECAL but phase and pulse width estimated by eye.







#### • Constant value simulation shows 200ns stabilization period.







• Ramp simulation shows almost fixed offset through voltage range.











### Acquisition Preamplifier



#### • OTA macromodel based double preamp design with 10x gain ratio.





### Gain Selection Comparator



#### • Comparator macromodel with tunable hysteresis and ideal components.





### Analog Multiplexer



• Multiplexer macromodel with ideal components.







#### • Testbench developed for the full channel ...







#### • but DC fails due to singular matrix in several blocks.







#### • Failing blocks are different and in separate signal paths.







• In all cases the issue is at the OTA macromodel ...







#### • specifically with the last source isolating the output from the dynamics.







# Thanks a lot for your attention!





# BACKUP



# PZ Cancellation Shaper Poly



#### • Polystyrene shape almost fits clock period, but weird tail effect.







#### • GFAG shape not fully available, but shaper reaches 25ns.







#### • Expected linear capacitor load but missing OTA saturation.









#### • Unity gain fitted for $\sigma$ =10ns gaussian centered in clock cycle.







#### • Constant value simulation shows 200ns stabilization period.









• Ramp simulation shows almost fixed offset through voltage range.

